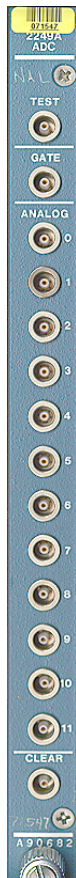# CAMAC Model 2249A 12 Channel A-to-D Converter

The LRS Model 2249A 12-Channel Analog-to-Digital Converter embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including expanded resolution (0.1%), higher sensitivity, excellent stability, faster digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

These ADCs are specifically intended for use in demanding applications such as particle identification using de/dx counters, recording x-ray, neutron, or recoil proton energies using lead glass or other total energy absorbtion counters, improving time resolution by correcting for slewing due to var- iances in counter output amplitudes, monitoring gas threshold Cerenkov counters, and debugging or monitoring proportional or drift chambers.

The Model 2249A contains twelve complete ADC's in a single-width CAMAC module. Each ADC offers a resolution of ten bits to provide 0.1% resolution over a wide 1024-channel dynamic range. The factor of 4 wider range allows operations with broad signal spectra such as are encountered in experi- ments anticipating fractionally charged particles or covering extensive energy ranges. It also greatly reduces the necessity for careful adjustment of signal strengths to match the limited range of an 8-bit, 256-channel instru- ment. The input sensitivity of the Model 2249A is 0.25 pC/count for a full-scale range of 256 pc. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by the unique test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into Pi, P2 or P5 of the Dataway connector.

The Model 2249A offers excellent event rate capability through the incorpo- ration of a fast clear and a fast digitizing rate. The fast clear input enables the ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information.This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

SPECIFICATIONS Model 2249A 12 CHANNEL ADC

Analog Inputs:	Twelve; Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ohm impedance; linear range normally -2 mV to - 1 V; protected to +/- 50 volts against 1 usec transients.
Full-Scale Range:	256 pC +/- 5%.
Full-Scale Uniformity:	+/- 5%.

Integral Non-linearity:	+/-.25% of reading +/- 0.5 pC (12 pC to 256 pC) for > 500 Ohm source.
ADC Resolution:	10 bits actual, (0.1%).
Long-Term Stability:	Better than 0.25% of reading +/- 0.5 pC/week (at constant temperature).
Temperature Coefficient:	Typical, 0; max., +/- [.03% of reading (in pC) + .002t] pC/'C (where t = gate duration in nanoseconds, with 50 Ohm reverse termination).
ADC Isolation:	A 5-volt, 20 ns overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.
Gate Input:	One gate common to all ADC'S; LEMO-type connectors; 50 Ohm impedance; - 600 mV or greater enables; minimum duration, 1 0 ns; maximum recommended duration, 200 ns (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5usec after opening gate to preserve accuracy), effective opening and closing times: 2 ns; internal delay, 2 ns.
Fast Clear:	One front-panel input common to all ADC'S; LEMO-type connector; 50 Ohm impedance; - 600 mV or greater clears, minimum duration, 50 ns. (Caution: narrower pulses cause partial clearing.) Requires additional 2.0 As settling time after clear.
Residual Pedestal:	Typically 1 + 0.03t picocoulombs (where t = gate duration in nanoseconds) with 50 Ohm reverse termination.
Test Function:	With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to + 12 volts) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of - 12.5 pC/volt into all inputs at F(25) . S2 time. (With CAMAC I not present, F(25) - S2 will generate the ~80 ns gate only, providing a measure of residual pedestal only.)
Digitizing Time:	60 us. By factory option, 8-bit operation at 12.5 us digitizing time may be provided.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 1 0 binary bits plus overflow bit of the selected channel onto the R1 to R1 1 (20 to 210) Dataway bus lines.
CAMAC Commands:	
Z or C:	ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM.
1:	Gate input is inhibited during CAMAC "Inhibit" command. (Test Function is enabled.)
0:	A Q = 1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q =0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.)

X:	An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is generated.
L:	A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	
F(0):	Read registers; requires N and A, A(0) through A(1 1) are used for channel addresses.
F(2):	Read registers and Clear module and LAM; requires N and A; (Clears on A(1 1) only.)
F(8):	Test Look-At-Me; requires N and any A from A(0) to A(l 1) independent of Disable Look-At-Me. Q response is generated it LAM is set.
F(9):	Clear module and LAM; requires N, S2, and any A from A(0) to A(11).
F(10):	Clear Look-At-Me; requires N, S2, and any A from A(0) to A(11).
F(24):	Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11).
F(25):	Test module; requires N, S2, and any A from A(0) to A(11).
F(26):	Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied.
Caution: The state of the LAM mask will be arbitrary after power turn-on.	
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered usefull. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.