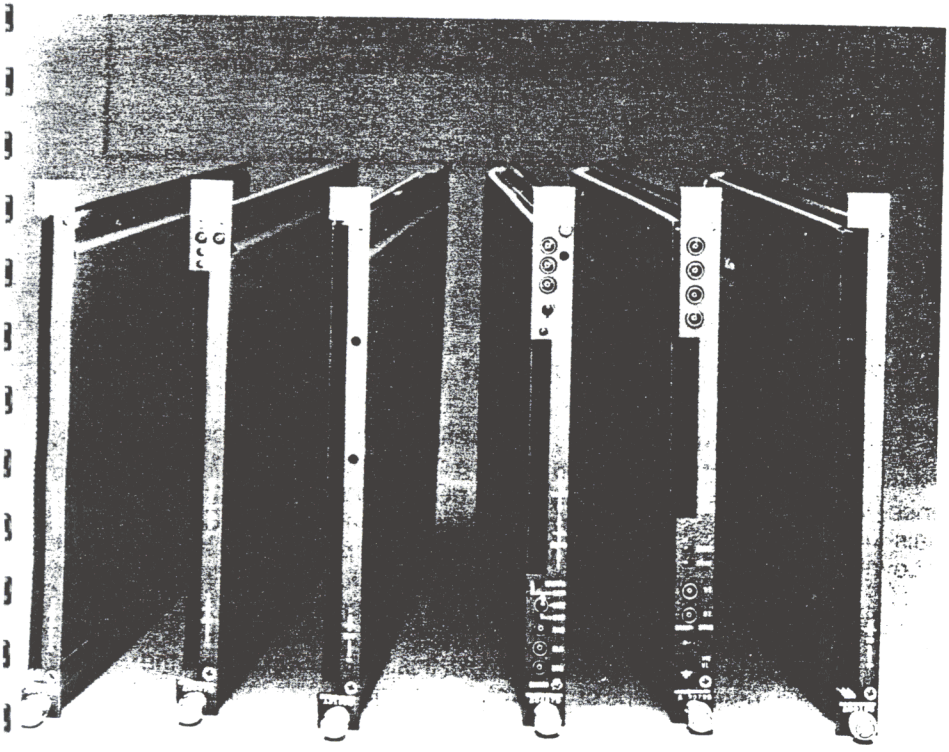
CAMAC ECLine
MODEL 4532
32 INPUT MAJORITY
LOGIC UNIT
USER'S MANUAL

October 1982

ECLine/CAMAC
Programmable First Level Trigger Modules

4418 PROGRAMMABLE LOGIC DELAY/FAN-OUT
4504 FLASH ADC
4508 PROGRAMMABLE LOOKUP UNIT
4516 PROGRAMMABLE LOGIC UNIT
4532 MAJORITY LOGIC UNIT
4564 OR LOGIC UNIT



- **High Speed First Level Trigger Decisions**
- **Programmable Logic Functions**
- **Compatible with ECLine Data Handler Modules**
- **Compatible with ECLine Discriminators, ADC/TDC, and MWPC Systems**
- **Designed-in Expandability**

FAST, FIRST LEVEL TRIGGER PROCESSING

The LeCroy ECLine family of programmable logic modules include logic delays, Boolean logic and other functions vital for high speed trigger systems. It also includes fast table lookup permitting pre-programmed responses to digital data. Functions are performed in only a few tens of nanoseconds, permitting data to be screened prior to recording and increasing the sensitivity of the experiment.

FEATURES

High Speed - Maximum rates of 65 to 150 MHz , depending on module and programmed features.

Multiple Functions - Relative timing adjustable by programmable logic delay, Majority Logic and simple Boolean Logic (AND/OR) for coincident events, Programmable lookup for complex functions.

Fan-Out Capability - Use of ECL (Emitter Coupled Logic) levels provides outputs suitable for fan-out to several modules (termination resistors may need to be removed on inputs).

Use of Multichannel Differential ECL - Signals for economic, fast, noise immune interconnections.

FUNCTIONAL DESCRIPTION

LeCroy's ECLine family of programmable logic modules are designed to quickly characterize data so that a rough go/no-go decision can be made for further processing. For example, discriminators are employed to ensure that analog signals are of sufficient amplitude to be interesting, and to provide logic outputs of fixed duration. This stage is then followed by a coincidence latch which records the pattern of "interesting signals" that occur within the same time window. The First Level Trigger modules ensure that specific combinations of signals have occurred. (Information on Discriminators and Latches may be found on other ECLine Programmable Logic Data Sheets.)

This first stage of data handling can then either reject the event as uninteresting, or can pass data on for further processing. The more sophisticated line of ECLine Data Handling modules include data conversion, arithmetic operations, fast "do loop" type operations, and specialized pattern recognition/ interpretation. Information on LeCroy Data Handling modules may be found on the Data Handlers technical data sheet. All functions are programmable to provide complete computer control of the triggering and data acquisition systems.

The LeCroy ECLine modules are compatible with the sophisticated FERA (Fast Encoding and Readout ADC) analog and time interval digitizing systems, as well as with the PCOS III Multiwire Proportional Chamber System. For exceptional data rates and on-board event accounting, the ECLine modules are also compatible with the LeCroy FASTBUS Multiple Event Buffer Memory, Model 1892. This compatibility provides a convenient method of storing data from ECLine modules, combining data from ECLine and FASTBUS (IEEE-960) systems, and provides the exceptional speed and data handling capability of the FASTBUS Standard.

Model 4418
Logic Delay/Fan-Out

Fast, passive logic delays are of prime importance for allowing all signals to arrive simultaneously at a data acquisition module. The LeCroy Model 4418 has 16 passive, tapped delay lines, one for each input. Each delay is individually set by computer via CAMAC in 1, 2 or 4 nsec increments (depending on sub-model or "MOD" selected), over a range of fifteen increments. The selection directs an output to "view" a particular tap on the delay line. For example, this feature would give the user a means of accurately aligning signals in time to compensate for differences in cable lengths.

Deadtimeless operation at speeds up to 100 MHz is assured by using passive delay lines and ECL switches. This feature provides the reliability of cable delays together with the speed and fan-out of ECL circuitry. As an added feature, each output is present three places on the front panel to provide additional fan-out capability. The cost of this device rivals cable delays.

Model 4504
Flash ADC

Four independent 4-bit (plus overflow) Flash ADC's are incorporated in the Model 4504. The sampling rate is adjustable from 20 to 100 MHz via front-panel control. Alternatively, a front-panel strobe input can be used to externally control the sampling rate.

The 4-bit ECL outputs are accompanied by a strobe output signal to indicate that the outputs are valid. This feature provides a convenient means to strobe subsequent logic (for example, the Model 4508 Programmable Logic Unit) that uses the Flash ADC results. A front-panel VETO input is provided for disabling the unit during periods when no input data can be processed.

The most common use of the 4504 is as a multiple threshold discriminator . The input may be derived directly from the detectors themselves or the analog outputs of other ECLine modules (Model 4532 for example).

Model 4508
Programmable Lookup Unit

Two independent 8-bit Programmable Lookup Units (PLU's) are included in the Model 4508. Each unit has an 8-bit digital input and an 8-bit digital output. The unit functions as an 8-bit addressable RAM. The contents are pre-programmed via CAMAC by the user. Each 8-bit input is a RAM address, and each 8-bit output is the content of this addressed location.

Output patterns are programmed into the PLU for each of the 256 possible input patterns. This unit can act as a complex logic module , a programmable calibration unit, or it may control the actions of subsequent logic based on the input pattern and programmed lookup table.

Each section of the Model 4508 can operate in one of three modes: Shaped, Overlap or Continuous. In the Shaped Mode, the outputs are a pulse of duration set by a front-panel adjustment. The inputs must be accompanied by a front-panel Strobe input signal . In Overlap Mode, the output pulse width (on all 8 bits) equals the input width if the Strobe input signal arrives before the input. Finally, in Continuous Mode, the output width reflects the time coincidence between Strobe and the inputs pulses.

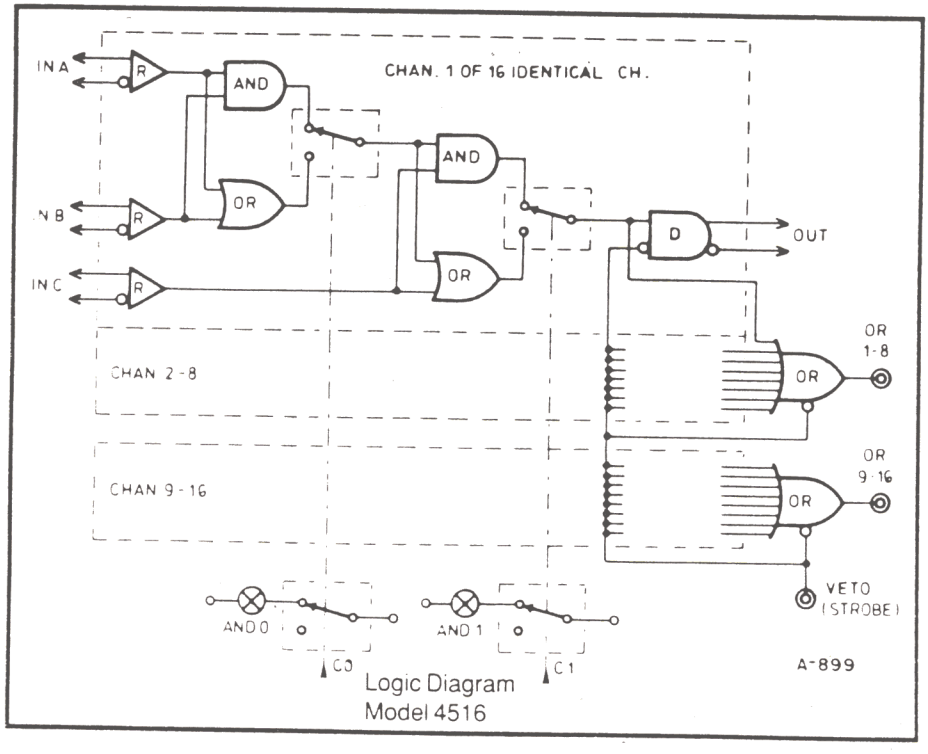
Model 4516
3-Fold AND/OR Logic Unit

Each of the 16 channels of the Model 4516 has three inputs (A, B and C). All channels have a front-panel output that is one of the Boolean combinations: (A•B•C), (A+B)•C, (A•B)+C, or (A+B)+C. The choice of logical function, AND(•) or OR (+), is set for all channels by two switches. These switches are set either by rear-panel manual switch settings or by computer command via CAMAC.

The 150 MHz speed of Model 4516 lends great versatility to this simple module. It can be used as a front-end AND/OR logic module, or an integral component in a higher level trigger processor.

Model 4532
Majority Logic Unit

Experiments that require a minimum number of signals to be present need a Majority Logic Unit. Each of the 32 inputs of the 4532 that is in a logical 1 state gives an incremental increase in a current sum output. An



Logic Diagram
Model 4516

onboard discriminator may then be used to signal when a user set current threshold (multiplicity) is exceeded. The current sum of each 4532 is available on two bridged outputs than permit daisy chaining of several modules. This feature extends the useful number of input sums by 32 inputs per daisy-chained module. For dynamic sampling, the analog output may be connected to an input of the Model 4504 Flash ADC. This unit provides a 4-bit digital output useful for trigger processing circuits.

The status of up to 32 inputs can be monitored and recorded by issuing a strobe. Since the inputs are edge-triggered, the strobe may be a gate of arbitrary duration. Then any inputs which are on during any portion of the gate are recorded and stored in a pattern register. The pattern register can then be read by computer via CAMAC. Alternatively, the 4532 can operate in Overlap Mode where the input pattern is not latched, and the outputs follow the inputs dynamically.

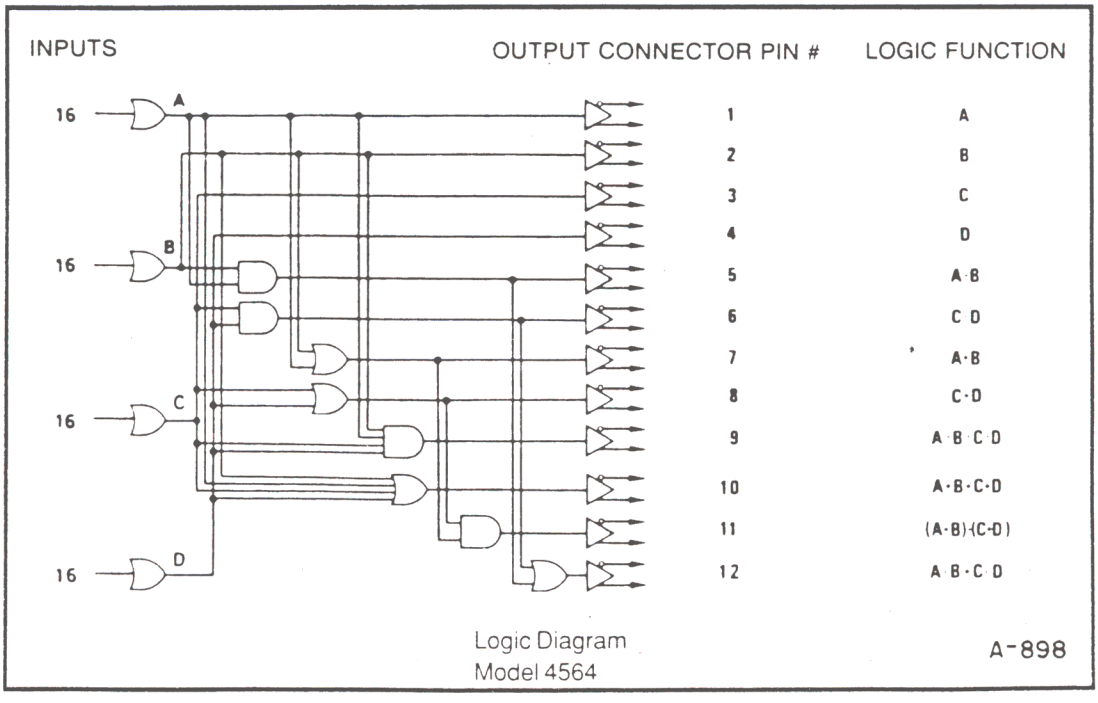
Other features of the Model 4532 are fast OR'ing of adjacent inputs, cluster mode operation, and provisions for cascading several 4532s for use in large detector arrays. Sixteen front-panel outputs give a fast OR output of inputs 1 and 2, 3 and 4, etc. These outputs reduce the number of signals that a second level trigger processor must view, while still maintaining a segmented set of signals. Next, in Cluster Mode, the 4532 will assume that adjacent hits indicate a single event and present only a single increment to the current output. This feature is useful in wire chambers where the close wire spacing often results in two or more adjacent wires giving signals from a single track. Finally, there is a provision for cluster Carry In and Carry Out to permit cascading several modules and permit cluster mode operation across module boundaries.

Model 4564
16 to 64 Fold OR Logic Unit

The Model 4564 is a simple and versatile logic module. It consists of four groups (A,B,C and D) of 16 input OR's followed by a set of additional 2 fold and 4 fold OR and AND functions. These various logic outputs, shown pictorially below, are simultaneously available on a rear-panel connector and the transit time is independent of the function. In addition, the outputs are capable of rates in excess of 100 MHz. Output width is dependent on the input pulse overlap.

For greater flexibility, the 4564 also offers four discriminator/ shaper channels. Internal jumpers allow any of the 12 logic combinations to be input to these channels. The output of discriminators/shapers can be triggered on the leading or tailing edge of the input (jumper selectable) and the width is adjustable from 15 nsec to greater than 500 nsec. Output polarity is also selectable via internal switches. These outputs can be used simply as an adjustable width logic fan-out or can allow for more sophisticated functions.

A typical application of the 4564 is to perform a simple track or pattern recognition for Veto or gate applications.



Logic Diagram
Model 4564

SPECIFICATIONS

Model 4418
Programmable Logic Delay/Fan-Out

Inputs: 16, DC coupled 100 Ω impedance, on 34-pin header for ECL signals. 100 MHz maximum rate (>35 MHz for Long Range Option), <10 nsec double pulse resolution (<30 nsec for long range option). Minimum width: 5 nsec.

Delay: 15-30 nsec in 1 nsec steps (4418/16), 15-45 nsec in 2 nsec steps (4418/32),15-135 nsec in 8 nsec steps (4418/128): Long Range Option. Delays set by computer for each channel individually.

Outputs: Three for each input, on three 34-pin headers, for compatibility with complementary ECL devices. Width equal to input duration ±1.2 nsec (±4 nsec Long Range Option). Risetime and falltime: 2.5 nsec.

Battery Back-Up: Preserves stored delays for at least 2 hours in the event of power loss.

Crosstalk: Synchronous pulses in adajcent channels can be affected by ±1 nsec typical.

Power: +6 V/50 mA, –6 V/2.5 A (15.3 W total)

Model 4504
Flash ADC

Inputs: Four on coaxial connectors, 50 Ω impedance, 10 nsec minimum width. Analog input range user defined between –2.5 V and +2.5 V. Range, set by computer command by giving low and high voltage reference levels, is divided by 15 to obtain resolution (4 bits).

Strobe: One ECL input for external strobe selected by front-panel switch. Leading edge initiates digitizing of all four inputs simultaneously; falling edge transfers digitized values to outputs and holds until next strobe. Maximum frequency 100 MHz. Alternate switch setting provides internal 20 MHz-100 MHz free-running strobe. Internal strobe frequency set by front-panel adjustment.

Veto: One ECL input inhibits strobe signal.

Outputs: Four, 4-bit ECL outputs on 8-pin headers. Overflow bits provided on 4 two-pin headers.

Strobe Out: Two on two-pin headers (ECL pulses) and two on Lemo connectors (–600 mV pulses) timed with digital outputs for downstream logic. Width is adjustable by front-panel potentiometer in the range of 5 to 25 nsec.

Test Points: Two front-panel test points permit measurement of voltage reference levels.

Input-Output Delay: Strobe trailing edge to digital outputs, typically 15 nsec.

Power: +6 V/1.1 A, –6 V/1.5 A, +24 V/6 mA (15.7 W total)

Model 4508
Memory Lookup Unit

Inputs: Two, 8-bit inputs on 34-pin header, 100 Ω for complementary ECL. Minimum width 10 nsec, maximum rate 65 MHz.

Strobe: Two on Lemo connectors, one per input section, 50 Ω impedance. Requires –600 mV signal, 5 nsec minimum width and must precede input by 2 nsec for exact time coincidence. Latches inputs, except in overlap mode. Maximum frequency >65 MHz. Strobe must be followed by clear except in Overlap Mode.

Clear: Two on Lemo connectors, one per input section, 50 Ω impedance. Requires –600 mV signal, 5 nsec minimum width to clear. Clears pattern register and resets outputs in all modes.

Outputs: Two, 8-bit outputs on 34-pin headers, ECL signals. Width of output in Shaped mode set by front- panel adjustment between <5 nsec to >100 nsec.

Synchro Output: Two on Lemo connectors, one per output section, 50 Ω impedance. Supplies –600 mV pulse out when outputs are ready. Typically used for strobing next unit, or for self-clearing.

Modes: Overlap (OVL) - Output pulse width determined by coincidence between Inputs and Strobe.

Shaped (SHP) - Output pulse width is determined by a front - panel adjustment from <5 to >100 nsec. The unit must be cleared before another input can be latched.

Continuous (CNT) - Output state is latched by the Strobe, until a Clear is applied.

Propagation Delay: (17 ±3) nsec in Overlap Mode. In other modes (21 ±1) nsec independent of logic function and determined by Strobe timing.

Power: +6 V/0.5 A, –6 V/2.6 A (18.6 W total)

Model 4516
Programmable Logic Unit

Inputs: 16 sets of three inputs, 100 Ω (high impedance by removal of socketed terminators), DC coupled, on 34-pin headers, for ECL signals, minimum 2 nsec risetime. Maximum rate 150 MHz.

Veto: One rear-panel Lemo connector, 50 Ω impedance. Requires –600 mV signal. Permits gating of outputs, including OR outputs. Must overlap coincidence for the three front-panel inputs by >5 nsec.

Outputs: 16, one per set of three inputs, complementary ECL logic levels on 34-pin header.

OR Out: Two, one for OR of first 8 outputs, one for second 8 outputs (factory option permits OR'ing of all 16 outputs).

Double Pulse Resolution: 5 nsec at minimum input width.

Coincidence Width: >3.5 nsec determined by input pulse width.

Input-Output Delay: A or B to OUT by 11 nsec typ.; A or B to OR by12 nsec, typ.; C to OUT by 8 nsec, typ.; C to OR by 9 nsec typ.; VETO to OUT by 8 nsec typ.; VETO to OR by 6 nsec typ.

Power: +6 V/50 mA, –6 V/1.25 A (7.8 W total)

Model 4532
Majority Logic Unit

Input : All inputs accept differential ECL level (–0.8 V, –1.7 V) into 110 Ω input impedance (high input impedance is possible by removing socket-mounted terminators).

Data Input (IN): 32 in two 34-pin front-panel connectors; minimum input pulse width 6 nsec.

Reset Input (RTI): Fast reset of the input registers; generates a reset of the analog majority output and of the comparator outputs (MDO, DMO). When the analog output is cascaded with other units, the RTI resets only the contribution from the modules that received the RTI. Minimum input pulse width 6 nsec, maximum width DC. In Memory Disable mode, the RTI is inhibited.

Gate Input (GAI): Normally open when unconnected. Normally closed when connected to a cable providing standard ECLine levels. In Memory Disable Mode, data pulses having an overlap with the GAI will contribute to the outputs. In Memory Enable Mode, data pulses having their leading edge inside the GAI time will be accepted and stored. By deriving the GAI from the DMO, an internally generated time window is possible. Minimum overlap time width with input pulses for majority decisions, 10 nsec. Minimum overlap time width with input pulses for logical OR's, 3 nsec, maximum width DC.

Cluster Carry (CCI): When Cluster Selection is Enabled, receives the carry information on the cluster from the Cluster Cary Output (CCO) of any adjacent majority logic unit.

Analog Majority Inpt/Output (AMIO): High impedance current source; AMIO connectors can be used for daisy chaining of analog majority information within a unit. Transit time between AMIO connectors 2 nsec. Unused output must be terminated with 50 Ω.

Output: All logic outputs provide complementary ECL levels (–0.8 V, –1.7 V) and are capable of driving differential 110 Ω loads.

Data Outputs (OUT): 16 in a 34 pin front-panel connector. In Memory Disable Mode, provides pulses corresponding to an overlap coincidence between the gate pulse and the data inputs. In Memory Enable Mode, provides levels started by the coincidence between the gate pulse and the leading edge of the data pulses.

OR Output (ORO): Provides the logical OR of the 32 channels, otherwise behaves as data outputs.

Strobe Output (STO): Provides a pulse, suitable for strobing of subsequent logic units, at the end of the gate input and delayed by the internal transit time (6 nsec). Width adjustable from 10 to 25 nsec by a trimmer (STROBE WIDTH) accessible from the side of the module.

Majority Discriminated Output (MDO): The AMIO input/output is internally used as input to an adjustable threshold comparator providing the MDO output. Threshold adjustable from 1 to 16 hits by a front-panel potentiometer (MA THR). The output will be a pulse or a level depending on the selected operating mode.

Delayed Majority Output (DMO): Reproduces the output MDO above, after an adjustable delay. A switch on the side of the module (DM RANGE) selects one of two delay ranges: 10-100 nsec or 50-1000 nsec. A front-panel potentiometer (DMO DELAY RANGE) permits continuous adjustment. The DMO is cleared as soon as the MDO is cleared.

Cluster Carry (CCO): When Cluster Selection is Enabled, indicates that Output channel 32 was hit for use in conjunction with channel 1 of a logically adjacent cluster logic in another 4532 module (CCI) input.

Mode Selection: A Memory Enable switch, accessible on the side of the module, selects one of the following modes: Memory Disable - Functions are disabled; the multiplicity calculation is performed on theoverlap of the data inputs. Memory Enable - The data inputs are latched; the multiplicity is determined by the number of leading edges of data input pulses occurring during the gate time. In this mode the unit needs to be cleared either by the reset input (RTI) or by a resetting function.

Cluster Slection: The Cluster Enable switch, accessible on the side of the module, determines one of the two following modes: Cluster Disable - Each data input provides one hit on the Analog Majority Output AMIO; the Cluster Carry Input (CCI) is disabled; Cluster Enable - Any group of adjacent input data pulses will be considered as a single hit. Provision has been made for the clusters to extend beyond the 32 inputs. If an input is present on the logically adjacent channel to input 1 of this unit but is located in another unit, the CCI can be used to indicate its presence. The CCO of this module indicates that channel 32 of this module is present.

Input-Output Delay: Data IN to AMIO - 16 nsec; AMIO to MDO output - 5 nsec; End of gate IN to Strobe OUT by 6 nsec; Data IN to Data OUT by 12 nsec; Data IN to OR OUT by 16 nsec; Reset IN to Data OUT by 20 nsec; Reset IN to OR OUT by 24 nsec; Data IN 32 to Cluster Carry OUT by 11 nsec; Cluster Carry IN to Data IN 1 by 2 nsec. Gate pulse must precede Data pulse by at least 7 nsec.

Power: +6 V/200 mA, –6 V/<3.6 A, +24 V/ 5 mA, –24 V/7 mA (23 W total).

Model 4564
16 to 64 Fold OR Logic Unit

Inputs: 64 in four 2 x 17 front-panel connectors, 110 Ω impedance. Minimum width 6 nsec, maximum frequency >100 MHz.

Overlap Outputs: Rear-panel 2 x 17 pin connector, pins 1 to 12, ECL signals. Width corresponds to overlap (±2 nsec) of inputs of logic function. minimum output 5 nsec, maximum output frequency >100 MHz; transit time 12 nsec ±1 nsec typical, independent of logic function; double pulse resolution 10 nsec typical.

Shaped Outputs: Rear-panel connector pins 13 to 16, any of overlap logic can be converted via jumper option to any of the four discriminator/shapers, output is differential ECL levels and width is internally adjustable from 15 to >500 nsec, can be triggered in leading or trailing edge of inputs (jumper selectable); output polarity internally switch selectable; maximum frequency: 30 MHz, double pulse resolution: 33 nsec.

Power: +6 V/150 mA, –6 V/1.5 A, –24 V/20 mA (10.4 W total)

CAMAC COMMANDS, FUNCTION CODES AND RESPONSES

Model 4418 Programmable Logic Delay/Fan-Out

F16•(A0 to A15):	Load delay time setting on write lines W1 to W4. One subaddress for each channel.
X, Q:	An X and Q response are generated when a valid N, A, F command is recognized.

Model 4504 Flash ADC

F(0)•A(0):	Read digital outputs; R1 to R16, 4 bits per channel.
F(0)•A(1):	Read digital overflow, R1 to R4, 1-bit per channel.
F(16)•A(0):	Write Low Reference Voltage (VL) on 8 bits; range from –2550 mV to +2250 mV in steps of 20 mV.
F(16)•A(1):	Same as above but for the High Reference Voltage (VH).
F(25)•A(0,1):	Equivalent to C.
C:	Generates a strobe during S2 time. This function is not affected by I or VETO input and may be disabled by a side-panel switch. The digital outputs will be set depending on the analog value of the inputs; in particular, if the inputs are disconnected all the digital outputs will correspond to 0 V at the inputs. The output logic state will be determined by the VL and VH reference voltages.
I:	Inhibit strobe.
X, Q:	X=1 and Q=1 responses are generated for any of the above functions.

Model 4508 Programmable Lookup Unit

F(0)•A(0):	Read first section 8-bit input pattern.
F(0)•A(1):	Read second section 8-bit pattern.
F(0)•A(2):	Read first section memory content at the given address; the memory content is displayed on read lines R1-R8, the given address on read lines R9-R16.
F(0)•A(3):	As F(0)•A(2) but for the second section.
F(2)•A(0):	Read first section 8-bit pattern and reset at S2; reset output levels when operating in continuous mode.
F(2)•A(1):	Same as F(2)•A(0), but for the second section.
F(2)•A(2):	Read first section memory content at the given address (as for F(0)•A(2)) and increment address by one at S2.
F(2)•A(3):	Same as F(2)•A(2), but for the second section.
F(9)•A(0):	Clear first section pattern; reset first section output levels when operating in continuous mode.
F(9)•A(1):	As above, but for the second section.
F(9)•A(2) or F(9)•A(3):	Reset memory address in both sections.

F(16)•A(0):	Load first section memory content at the given address; data have to be sent on write lines W1-W8;
F(16)•A(1):	As above, but for the second section.
F(16)•A(2):	Random access to the first section memory (the selected address has to be sent on write lines W9-W16); load memory content with data present on W1-W8, at the selected address.
F(16)•A(3):	Same as above, but for the second section.
F(18)•A(0):	Load first section memory content, at the given address, with data present on W1-W8; increment address by 1.
F(18)•A(1):	As above, but for the second section.
F(18)•A(2) or F(18)•A(3):	Load the memory's address register (this address has to be sent on write lines W9-W16).

Z or C:	The address register for the memories of both sections is set to 0; pattern registers are cleared.
X:	An X=1 response is generated for any valid CAMAC function.
Q:	A Q=1 response is generated for any valid CAMAC function, except when the memory addresses overflow. (This latter feature permits one to recognize when the reading or the loading of a memory has been completed).

Model 4516 Programmable Logic Unit

F(26)•A(0):	Sets all C0's to AND Mode.
F(24)•A(0):	Sets all C0's to OR Mode.
F(26)•A(1):	Sets all C1's to AND Mode.
F(24)•A(1):	Sets all C1's to OR Mode.
F(27)•A(0):	Gives a Q response if C0 switch is in AND Mode.
F(27)•A(1):	Gives a Q response if C1 switch in in AND Mode.

X:	An X response is generated when a valid N, A, F command is recognized.
Z:	Sets all channels to OR Mode.

Model 4532 Majority Logic Unit

F(0)•A(0), A(1):	Read input pattern. A(0): channels 1 to 16. A(1): channels 17 to 32. A Q response is generated in Memory Enable Mode only.
F(1)•A(0):	Read status register; R1 = 1 if LAM isON; R2 = 1 if LAM Enable switch is ON; R3 = 1 if MEMORY Enable switch is ON; R4 = 1 if CLUSTER Enable switch is ON. Q response is always generated.
F(2)•A(0):	Read input pattern, channels 1 to 16. Q response is generated in Memory Enable Mode only.
F(2)•A(1):	Read input pattern, channels 17 to 32, and clears the 32-channel memory and LAM at S2. Q response is generated in Memory Enable Mode only.
F(8)•A(0):	Test LAM; a Q response is generated if L is ON.
F(9)•A(0):	Clears the data memory and LAM.
F(10)•A(0):	Test and clear LAM, clears LAM . Q response is generated if L is ON. The clear LAM operation is not executed if Q response is missing.

Z, C:	Clears data memory and LAM .
L:	A Look-At-Me signal is generated (in Memory Enable Mode only) at the end of the gate input if the OR output is set. The LAM may be enabled or disabled by the LAM enable switch accessible on the side of the module.
X:	An X=1 response is generated for any executable function.
Q:	A Q=1 response is generated for any executable function in Memory Enable Mode only.

Model 4564 OR Logic Unit - The Model 4564 does not utilize CAMAC Commands or Function Codes.

GENERAL DESCRIPTION

The LeCroy Model 4532, Majority Logic Unit, has two basic modes of operation depending on the position of the MEMORY ENABLE switch.

If the MEMORY ENABLE switch is OFF, the 4532 is completely transparent with respect to inputs and outputs.The information present at all outputs will be a function of the instantaneous signals at the inputs during the gate time. The CAMAC functions become clearely meaningless, and will not be executed. No Q response will be generated.

If the MEMORY ENABLE switch is ON, pulses arriving at the input having their leading edges falling during the GATE pulse widths, will be stored.

Consequently, at the end of the GATE pulse, all the outputs will be stable and a LAM signal can eventually be generated. The information at the outputs will remain stable until a reset is applied either by CAMAC or by the input RTI (Reset Input).

It should be noted that the RTI input does not clear the LAM. This avoids problems during the CAMAC search for LAM sources.

On the other hand, the RTI input cleares the data memory. Therefore care should be taken to synchronisation the CAMAC activity with with the RTI signals.

FUNCTIONAL DESCRIPTION

The following description refers to the bloc diagram and schematics included with this manual. Depending on the operation mode, the input pulses can either set bits in a memory or go through an AND gate enabled by the GATE input.

After this initial stage, the signals coming either from the memory or from the AND gate, follow same path. These signals are termed "internal data", and pass through the following consecutive logic stages.

1. OR outputs

   The module provides a general logical OR of the 32 internal data on the output connector ORO (OR Output). In addition, the logical OR of the internal data taken 2 by 2 (IN1.OR.IN2 on OUT1, IN3.OR.IN4 on OUT2, and so on) is generated on the OUTs 1 to 16.

2. Cluster logic

   If the CLUSTER ENABLE switch is OFF, the 32 channels of internal data go directly to the Digital to Analog Converter (DAC) which sets the multiplicity analog level at the output. If the CLUSTER ENABLE switch is ON, each internal data vetoes the adjacent higher one. Consequently only the first bit in a set of consecutive bits (cluster) will be active into the DAC.

   In order to cascade several 4532's, channel 1 can be vetoed by the Cluster Carry Input (CCI). The internal data present on channel 32 is provided for the next 4532 module on the Cluster Carry Output (CCO).

3. Analog Majority Input-Output (AMIO)

   After the cluster logic the data is converted to a current by the DAC.

   The presence of a bit in the data coming into the DAC generates a 1.6 mA current source (adjustable by changing the Voltage-VD) in circuitry which at the same time adds these currents.

   The sum of the currents is performed by the common base mounted transistors T1 and T2.

The collectors of T1 and T2 are connected together to finally give the total sum of the currents. This total current is carried to the base of transistor T12 and the collector of transistor T3.

The current flowing through T4 and T12 will be the image of the one flowing through T3. This fact permits the transfer of the current to T5, T13 and T6, mounted in the same configuration as T3, T4, T12.

The resistance on the T6 emitter is one half of the one on the T5 emitter. This means that the current finally procided by T3 at the output, will be of 3.2 mA/hit. In order to compensate the different offset currents that can be present, the transistor T7 produces a constant current, adjustable by the internal potentiometer OADJ (offset adjustement), permitting a zero quiescient current on AMIO.

The circuitry is protected against missing 50 Ω terminations at the AMIO outputs, by the 39 Ω resistor between T12 and T5.

4. Majority Discriminated Output (MDO)

The AMIO signal is directly connected to a comparator input. The comparator threshold can be adjusted between O V and -1.5 V by the front panel potentiometer MATHR (Majority Threshold). It should be noted that the status of MDO output will be conditioned not only by the DAC output, but also by signals connected to the AMIO from other units.

5. Delayed Majority Output (DMO)

The output DMO is internally connected to a delay circuit based on the principle of a comparator connected to a capacitor being charged by a constant current. The comparator threshold, and resulting delay, can be adjusted by the front panel potentiometer DM DEL. The digital output of comparator MDO regulates the charge and discharge of this capacitor. When the MDO is off the transistor T8 discharges and holds the capacitor at a high reference voltage. When the MDO comparator provides a signal, T8 goes off and the capacitor charges with constant current and the amplitude of this charge is limited by T9.

The DM DEL switch selects two capacitor values to permit two different delay ranges.

6. Strobe Output (STO)

The width of the strobe output is determined by the charge at constant current of the variable capacitor ST WIDTH. When a gate signal GAI is applied, it closes the gate B1 and charges the variable capacitor. The amount of the charge is limited by T10 and T11. At the end of the gate pulse, B1 opens again and the variable capacitor discharges. The strobe output STD will be present as long as the voltage on the variable capacitor is greater than the threshold of B1.

It should be noted that STO is cleared by GAI and starts again from the end of GAI.

7. LAM circuit

LAM circuit is composed of the two flip-flops I1. The first one memorizes a LAM request and acts on the L line. Its setting is dependent on switches LAM ENABLE and MEMORY ENABLE being ON. The first flip-flop is set by the leading edge of the signal provided by gate B1, pin 14, and translated by transistor T12.

Gate B1 has the function of halting the OR signal during GAI which would have generated a LAM.

The second flip-flop, which is coupled to the first one, is set at the beginning of a CAMAC cycle if the L line is ON. It generates the Q response in recognition of F(8) and F(10).

In order to avoid loss of a LAM request coming during F(10), the reset by F(10) is halted if a Q response has not been delivered.