Acromag®

Series IP408 Industrial I/O Pack
32-Channel Digital I/O Board

USER'S MANUAL

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DRAWINGS

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP408 module is a 32-channel combination digital input/output board. This model supports both 0 to 60V DC inputs, and 60VDC low-side switch outputs, in any combination up to 32 channels. Four units mounted on a carrier board provide up to 128 I/O points per 6U-VMEbus system slot. As a combination input/output module, input channels on this model can be used for "loopback" monitoring of the output channel states. Up to 8 input channels can be programmed to generate Change-Of-State (COS), Low, or High level transition interrupts. The IP408 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for a wide range of industrial control and monitor applications that require high-density, high-reliability, and high-performance at a low cost.

KEY IP408 FEATURES

- **High Channel Count** - Interfaces with up to 32 input/output points. Four units mounted on a carrier board provide up to 128 input and/or output channels in a single system slot. Input and output channels may be intermixed in any combination. The input circuitry of a single channel can also be used to monitor the output state of the same channel to efficiently implement "loopback" output control.
- **TTL-Compatible Input Threshold** - Input threshold is at TTL levels and includes hysteresis.
- **Input Hysteresis** - Buffered inputs include hysteresis for increased noise immunity.
- **Programmable Change-of-State/Level Interrupts -** Interrupts are software programmable for any bit Change-Of-State or level on up to 8 channels.
- **Loopback Output Control & Fault Diagnostics** - Input and output circuitry is connected in tandem to each I/O channel, making it directly compatible for "loopback monitoring" of the output channel states. This feature can also be used to implement self-test or fault diagnosis, since inherent loopback can be used to detect open output switches or shorts.

- **High Voltage Inputs & Outputs** - Inputs and outputs are rated to 60VDC. I/O channels are non-isolated and share a common connection.
- **High Impedance Inputs** - High impedance inputs minimize loading of the input source and input current.
- **No Configuration Jumpers or Switches** - All configuration is performed through software commands with no internal jumpers to configure or switches to set.
- **Power Up & System Reset is Failsafe** - For safety, the outputs are always OFF upon power-up and cleared after a system reset. Unlike some competitive units, output gate pulldowns are included to ensure that the outputs do not turn on momentarily when output load power is applied with no power to the IP module.
- **True Logic** - Outputs operate using True-Logic (1=ON/SWITCH CLOSED, 0=OFF/SWITCH OPEN).
- **Low R_{dsON} (0.2Ω Maximum)-** Low output drain-to-source ON resistance ensures TTL logic-low compatibility at high currents and reduces power dissipation.
- **High Output Current** - individual output channels may sink up to 1A DC continuous (up to 10A total, all channels combined), or 312mA DC (with all 32 channels ON). No deration of maximum output current is required at elevated ambient temperatures.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry-standard, IP module footprint. Up to four units may be mounted on a 6U VMEbus carrier board.
- **Local ID** - Each IP module has its own 8-bit ID PROM which is accessed via data transfers in the "ID Read" space.
- **16-bit & 8-bit I/O** - Channel register Read/Write is performed through D16 or D08 (EO) data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states. For Model IP408, only 1 wait state is required for read and write operations (see specifications for detailed information).

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent carrier boards). Consult the documentation of your carrier board to ensure compatibility with the following interface products (since all connections to field signals are made through the carrier board which passes them to the individual IP modules).

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Termination Panel:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from the card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette to simplify communication with the board (Model IPSW-LIB-M03, MSDOS format). All functions are written in the "C" programming language and can be linked to your application. Refer to the "README.TXT" file in the root directory and the "INFO408.TXT" file in the "IP408" subdirectory on the diskette for more details.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Model IP408 I/O Boards have no jumpers or switches to configure--interrupts are configured through software command.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

Table 2.1: IP408 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
OD00	1	OD25	32
OD01	2	OD26	33
OD02	3	OD27	34
OD03	4	OD28	36
OD04	6	OD29	37
OD05	7	OD30	38
OD06	8	OD31	39
OD07	9	***Not Used***	41
OD08	11	***Not Used***	42
OD09	12	***Not Used***	43
OD10	13	***Not Used***	44
OD11	14	***Not Used***	46
OD12	16	***Not Used***	47
OD13	17	***Not Used***	48
OD14	18	***Not Used***	49
OD15	19	COMMON	5
OD16	21	COMMON	10
OD17	22	COMMON	15
OD18	23	COMMON	20
OD19	24	COMMON	25
OD20	26	COMMON	30
OD21	27	COMMON	35
OD22	28	COMMON	40
OD23	29	COMMON	45
OD24	31	COMMON	50

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the front-panel, field-I/O interface connector on the carrier board (you should verify this for your carrier board). The P2 pin assignments of the IP408 I/O module correspond with those of the IP400 input module and the IP405 output module (for channels 0-31 and common).

I/O Noise and Grounding Considerations

The output channels of this model are the open drains of mosfets with a common source connection. The IP408 is non-isolated between the logic and field I/O grounds since output common is electrically connected to the IP module ground. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Two ounce copper ground plane foil has been employed in the design of this model to help minimize the effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

This device is capable of switching many channels at high currents. Additionally, the nature of the IP interface is inherently inductive. The outputs of this model are protected to voltages up to 60V. As such, when switching inductive loads, it is important that careful consideration be given to the use of snubber devices to shunt the reverse emf that develops when the current through an inductor is interrupted. Filtering and bypassing at the load may also be necessary. Additionally, proper grounding with thick conductors is essential. Interface cabling and ground wiring should be kept as short as possible. For outputs, the use of an interposing relay may also be desireable for isolating the load, raising the drive capability, or providing additional system protection. Please refer to Drawing Drawing 4501-520 & 4501-522 for examples of these connections and proper output and grounding connections.

Output Off-State Loading Considerations

With respect to output control, the 100KΩ input buffer current-limiting resistors in combination with +4.7V voltage clamps will tend to increase the off-state drain current with increased drain voltage (up to 0.5mA at 60V). This is due to the fact that the input buffer circuitry and output mosfet drain circuitry are connected in tandem to the same I/O pin. If this presents a problem for your application, then you should consider separating the inputs and outputs by using other IP modules like the Acromag IP400 40-channel input board and the IP405 40-channel output board.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). Note that the IP408 does not utilize all of the logic signals defined for the P1 connector and these are indicated in ***BOLD ITALICS***.

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the ON/OFF states of individual low-side switches and/or the acquisition of digital inputs from the field. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP408 only uses a portion of this space. The I/O space address map for the IP408 is shown in Table 3.1. Note the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. Accesses can be performed on an 8-bit (D08[EO]), or 16-bit (D16) word basis.

Table 3.1: IP408 I/O Space Address (Hex) Memory Map

EVEN Base Addr.+	EVEN Byte D15 D08	ODD Byte D07 D00	ODD Base Addr.+
00	READ- Digital Input Channel Register A CH15 ↔ CH08	READ- Digital Input Channel Register A CH07 ↔ CH00	**01**
02	READ- Digital Input Channel Register B CH31 ↔ CH24	READ- Digital Input Channel Register B CH23 ↔ CH16	**03**
04	R/W -Digital Output Channel Register A CH15 ↔ CH08	R/W -Digital Output Channel Register A CH07 ↔ CH00	**05**
06	R/W - Digital Output Channel Register B CH31 ↔ CH24	R/W -Digital Output Channel Register B CH23 ↔ CH16	**07**
08	NOT DRIVEN	R/W - Interrupt Enable Register[1] CH07 ↔ CH00	**09**
0A	NOT DRIVEN	R/W -Interrupt Type Config. Register[1] CH07 ↔ CH00	**0B**
0C	NOT DRIVEN	R/W - Interrupt Polarity Register[1] CH07 ↔ CH00	**0D**
0E	NOT DRIVEN	R/W - Interrupt Status Register[1] CH07 ↔ CH00	**0F**
10	NOT DRIVEN	R/W - Interrupt Vector Register[1]	**11**
12 ↓ 7E	NOT USED[2]		**13 ↓ 7F**

Notes (Table 3.1):
1. The upper 8 bits of this register are not driven. Pullups on the carrier board data bus will cause these bits to always read high (1's).
2. The IP will not respond to addresses that are "Not Used".

IP Digital Input Registers A & B (Read Only)

When the Digital Input Channel Data Registers are read, the value read corresponds to the actual state of the input channels at the time of the read. If the channel's tandem output mosfet is being controlled and its drain is loaded, then reading the digital input channel data register will return the state of the output (it is directly connected to the drain). This is an efficient method of accomplishing "loopback" control of the output. A "0" bit means that the corresponding input signal is below the threshold value (or the tandem output mosfet is ON), a "1" bit means that the corresponding input signal is at or above the threshold value (or the tandem mosfet is OFF and pulled up).

Thirty-two possible input channels numbered 0 through 31 may be read. Channel read operations use 8-bit (D08(EO)), or 16-bit (D16) data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest (see below). Register A monitors input channels 0 through 15. Register B monitors input channels 16 through 31.

It is recommended that unused inputs not be left floating, but pulled low by turning on the corresponding tandem output (see IP Digital Output Registers).

REGISTER A (INPUT CHANNELS 0 THROUGH 15):

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH15							CH8	CH7							CH0

REGISTER B (INPUT CHANNELS 16 THROUGH 31):

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH31							CH24	CH23							CH16

IP Digital Output Registers A & B (Read/Write)

When the Digital Output Channel Data Registers are written to, the value written is represented at the corresponding output channels. A "0" bit means that the corresponding output switch is OPEN (OFF). Writing a "1" bit CLOSES the corresponding output switch (turns it ON). There are two ways to accomplish an output read. Reading the digital output channel register returns the state configuration of this register (which is equivalent to the output mosfet gate signal). Since input channels operate in tandem with the output channels, reading the digital input channel register will return the actual state of the output (it returns the level of the output mosfet drain). That is, writing a '1' to an output turns the switch ON (gate signal high). In turn, this drives the drain low (mosfet is conducting). As such, a read of the input channel register will be the inverse of a read of the output channel register for a loaded output channel.

Read/Write Control for 32 output channels numbered 0 through 31 is provided. Channel state Read/Write operations use 8-bit even or odd-byte (D08[EO]), or 16-bit (D16) data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest (see below). Register A controls output channels 0 through 15. Register B controls output channels 16 through 31.

REGISTER A (OUTPUT SWITCHES 0 THROUGH 15):

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH15							CH08	CH7							CH0

REGISTER B (OUTPUT SWITCHES 16 THROUGH 31):

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH31							CH24	CH23							CH16

Each output channel register can be conveniently read back for verification purposes. However, for critical control applications, it is recommended that outputs be directly fed back to input points and the input points monitored (loopback I/O). By design, input channels are tied to the drains of the tandem output mosfet and a read of the input channel register will return the inverse of a read of the output channel register (a read of the input returns the drain level, a read of the output returns the gate level). This is an efficient method of accomplishing loopback output control without requiring additional channels. However, this only applies for a loaded drain (a pullup or other load connected to the drain).

All outputs are OFF (switch OPEN) following a power-on reset, and are immediately cleared following a system reset. It is recommended that unused outputs be turned on so that the corresponding unused inputs are pulled low, rather than floating.

Interrupt Enable Register (R/W)

The digital input channel Interrupt Enable Registers provide a mask bit for each of the 8 possible interrupt channels (channels 0-7 only). A "0" bit will prevent the corresponding input channel from generating an external interrupt. A "1" bit will allow the corresponding input channel to generate an interrupt. The unused upper 8 bits of these 16-bit registers are "Don't Care" and will always read high (1's) for D16 accesses.

INTERRUPT ENABLE REGISTER:

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	CH7							CH0

All input channel interrupts are masked ("0") following a reset.

Interrupt Type (COS or H/L) Configuration Register (R/W)

The Interrupt Type Configuration Registers determine the type of input channel transition that will generate an interrupt for each of the 8 possible interrupt channels (channels 0-7 only). A "0" bit means that an interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A "1" bit means the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition). The unused upper 8 bits of these 16-bit registers are "Don't Care" and will always read high (1's) for D16 accesses. Note that interrupts will not occur unless they are enabled.

INTERRUPT TYPE (COS or H/L) CONFIGURATION REGISTER:

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	CH7							CH0

All bits are set to "0" following a reset which means that the inputs will cause interrupts for the levels specified by the digital input channel Interrupt Polarity Register.

Interrupt Polarity Register (R/W)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the 8 possible interrupt channels (channels 0-7 only). A "0" bit specifies that an interrupt will occur when the corresponding input channel is *BELOW* TTL threshold (i.e. a "0" in the digital input channel data register). A "1" bit means that an interrupt will occur when the input channel is *ABOVE* TTL threshold (i.e. a "1" in the digital input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

INTERRUPT POLARITY (HIGH/LOW) REGISTER:

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	CH7							CH0

The unused upper 8 bits of these 16-bit registers are "Don't Care" and will always read high (1's) for D16 accesses. All bits are set to "0" following a reset which means that the inputs will cause interrupts when they are below TTL threshold.

Interrupt Status Register (R/W)

The Interrupt Status Register reflects the status of the 8 possible interrupt channels (channels 0-7 only). A "1" bit indicates that an interrupt is pending for the corresponding channel. A channel that does not have interrupts enabled will never set its interrupt status flag. A channel's interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status Register (writing a "1" acts as a reset signal to clear the set state). This is known as the "Release On Register Access" (RORA) method, as defined in the VME system architecture specification. However, if the condition which caused the interrupt to occur remains, the interrupt will be generated again (unless disabled via the Interrupt Enable Register).

Note that interrupts are prioritized via hardware within the card. Channel 7 has the highest priority, channel 0 the lowest priority. If multiple input channel interrupts become pending at the same time, the vector corresponding to the highest numbered channel will be delivered first. After the highest numbered channel's interrupt is serviced and cleared, an additional interrupt will be generated for the next highest priority channel with an interrupt pending. Note that the input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a specific input channel, this could happen if multiple changes occur before the channel's interrupt is serviced.

INTERRUPT STATUS REGISTER:

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	CH7							CH0

All interrupts are cleared following a reset.

Interrupt Vector Register (R/W)

The Interrupt Vector Register maintains an 8-bit interrupt pointer for each of the 8 digital input channel interrupt lines (channels 0-7 only). The lower 3 bits of the Interrupt Vector Register (odd byte address) contain the channel number that originated the interrupt. The upper 5 bits of the odd-addressed byte are user-programmable and contain a pointer to the interrupt service routine. Interrupts are served on a priority basis with the higher numbered channels having higher priority (i.e. channel 7 has the highest priority, channel 0 the lowest). The appropriate interrupt vector is given to the VMEbus Interrupt Handler when an interrupt is being serviced. As such, it is a pointer to 8 possible interrupt handling routines. This allows each digital input channel to be serviced by its own software handler.

INTERRUPT VECTOR REGISTER:

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	User-Programmable					Channel No.		

All bits of this register are set to "0" following a reset.

IP ID PROM (Read Only, 32 odd-byte addresses)

Each IP module contains an identification (ID) PROM that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP408 ID PROM does not contain any variable (e.g. unique calibration) information. ID PROM bytes are addressed using only the odd addresses in a 64 byte block.

The IP408 ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM. Execution of an ID PROM Read operation requires 1 wait state.

Table 3.2: IP408 ID Space Identification (ID) PROM

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		03	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		C2	CRC
19 to 3F		yy	Not Used

Notes (Table 3.2):

1. The IP model number is represented by a two-digit code within the ID PROM (the IP408 model is represented by 03 Hex).

IP408 PROGRAMMING CONSIDERATIONS

To make programming and communicating with the board easier, Acromag provides you with the Industrial I/O Pack Software Library diskette. The functions provided are written in the "C" programming language and can be linked into your application. Refer to the "README.TXT" file in the root directory and the "INFO408.TXT" file in the "IP408" subdirectory on the diskette for details.

The following sections give some pointers for programming interrupts.

Programming Interrupts

Digital input channels can be programmed to generate interrupts for the following conditions (channels 0-7 only):

- Change-of-State (COS) at selected channels.
- Input level (polarity) match at selected input channels.

Interrupts generated by the IP408 use interrupt request line INTREQ0* (Interrupt Request 0). The interrupt release mechanism employed is the Release On Register Access (RORA) type. This means that the interrupter will release the Industrial I/O Pack interrupt request line (INTREQ0) after the interrupt has been cleared by writing a "1" to the appropriate bit position in the input channel Interrupt Status Register.

The Interrupt Vector Register contains a pointer to an interrupt handling routine. The lower 3 bits of this 8-bit number contain the channel number of the interrupting channel. The upper 5 bits of this 8-bit number contain a user-programmable pointer to complete the vector. As such, the vector may point to any one of 8 possible locations to access the interrupt handling routine. If each of these 8 locations contain the same address (the address of the interrupt handling routine), one interrupt handling routine may be used to service all possible channel interrupts.

Interrupt service is prioritized with the higher numbered channel having a higher priority over the lower numbered channels. Thus, Channel 7 has the highest priority and channel 0 the lowest. As such, if multiple channel interrupts become pending at the same time, the pointer corresponding to the highest numbered channel will be delivered first. After the highest numbered channel interrupt is serviced and cleared, an additional interrupt will be generated for the next highest priority (pending) interrupt.

When using interrupts, input channel bandwidth should be limited to reduce the possiblity of missing channel interrupts. For a given input channel, this could happen if multiple changes occur before the channel's interrupt is serviced. The response time of the input channels should also be considered when figuring this bandwidth. The total response time is the sum of the input buffer response time, plus the interrupt logic circuit response time, and this time must pass before another interrupt condition will be recognized.

The following programming examples assume that the IP408 is installed onto an Acromag AVME9630/9660 carrier board (consult your carrier board documentation for compatibility details).

Programming Example for AVME9630/9660 Carrier Boards:

1. Clear the global interrupt enable bit in the Carrier Board Status Register by writing a "0" to bit 3.
2. Perform Specific IP Module Programming - see the Change-of-State or Level Match programming examples that follow, as required for your application.
3. Write to the carrier board Interrupt Level Register to program the desired interrupt level per bits 2, 1, & 0.
4. Write "1" to the carrier board IP Interrupt Clear Register corresponding to the IP interrupt request(s) being configured.
5. Write "1" to the carrier board IP Interrupt Enable Register bits corresponding to the IP interrupt request to be enabled.
6. Enable interrupts from the carrier board by writing a "1" to bit 3 (the Global Interrupt Enable Bit) of the Carrier Board Status Register.

IP Programming Example for Change-of-State Interrupts:

1. Program the upper 5 bits of the odd-addressed byte of the Interrupt Vector Register with the user specified portion of the interrupt vector. These 5 bits combined with the lower 3 bits (the interrupting channel number) form a pointer to one of 8 possible locations in memory that contain the address of the interrupt handling routine.
2. Select channel Change-of-State interrupts by writing a "1" to each channel's respective bit in the Interrupt Type Register. Note that Change-Of-State interrupts (specified with "1") may be mixed with polarity match interrupts (specified with "0").
3. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Register.
4. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register.

   Change-of-State Interrupts may now be generated by the input channels programmed above for any Change-Of-State transition.

IP Programming Example for Level (Polarity) Match Interrupts:

1. Program the upper 5 bits of the odd-addressed byte of the Interrupt Vector Register with the user specified portion of the interrupt vector. These 5 bits combined with the lower 3 bits (the interrupting channel number) form a pointer to one of 8 possible locations in memory that contain the address of the interrupt handling routine.
2. Select channel polarity match interrupts by writing a "0" to each channel's respective bit in the Interrupt Type Register. Note that Change-Of-State interrupts (specified with "1") may be mixed with polarity match interrupts (specified with "0").
3. Select the desired polarity (High/Low) level for interrupts by writing a "0" (Low), or "1" (High) level to each channel's respective bit in the Interrupt Polarity Registers.
4. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Registers.
5. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register.

   Interrupts can now be generated by matching the input level with the selected polarity for programmed interrupt channels.

General Sequence of Events for Processing an Interrupt

1. The IP408 asserts the Interrupt Request 0 Line (INTREQ0*) in response to an interrupt condition at one or more inputs.
2. The AVME9630/9660 carrier board acts as an interrupter in making the VMEbus interrupt request (asserts IRQx*) corresponding to the IP interrupt request.
3. The VMEbus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.

4. When the asserted VMEbus IACKIN* signal (daisy-chained) is passed to the AVME9630/9660, the carrier board will check if the level requested matches that specified by the host. If it matches, the carrier board will assert the INTSEL* line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to IntReq0*; A1 high corresponds to INTREQ1* which is not supported by the IP408).
5. The IP408 puts the appropriate interrupt vector on the local data bus (D00-D07 for the D08 [O] interrupter) and asserts ACK* to the carrier board. The carrier board passes this along to the VMEbus (D08[O]) and asserts DTACK*.
6. The host uses the vector to form a pointer to an interrupt service routine for the interrupt handler to begin execution.
7. Example of Generic Interrupt Handler Actions:
   A. Disable the interrupting IP by writing "0" to the appropriate bit in the AVME9630/9660 IP Interrupt Enable Register.
   B. Disable the interrupting channel(s) by writing a "0" to the appropriate bits in the IP408 Interrupt Enable Register.
   C. Clear the interrupting channel(s) by writing a "1" to the appropriate bits in the IP408 Interrupt Status Register.
   D. Enable the interrupting channel(s) by writing a "1" to the appropriate bits in the IP408 Interrupt Enable Register.
   E. Clear the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/9660 IP Interrupt Clear Register.
   F. Enable the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/9660 IP Interrupt Enable Register.
8. If the IP408 interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle is complete (i.e. the carrier board negates its interrupt request, IRQ*).
   A. If the IP408 interrupt stimulus remains, a new interrupt request will immediately follow. If the stimulus cannot be removed, the IP408 should be disabled or reconfigured.
   B. If other IP modules have interrupts pending, then the interrupt request (IRQx*) will remain asserted. This will start a new interrupt cycle.

4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown in Drawing 4501-521 as you review this material.

INPUT/OUTPUT

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Field I/O points are NON-ISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawings 4501-520 & 4501-522 for example I/O and grounding connections.

A Field Programmable Gate Array (FPGA) is used to generate all the logic necessary to operate the board. With respect to input acquisition, the interrupt channels drive the FPGA through 8 individual buffers (channels 0-7 only). The input buffers of the other 24 channels are selectively enabled and drive the data bus directly. The field input signals are tied to the inputs of these buffers via a 100KΩ series connected resistor which limits the input current (but raises the tandem output's off-state drain current). Additionally, the buffer inputs are clamped to +4.7V (generated from the +12V supply to minimize +5V loading). The input signal threshold is TTL compatible. The typical threshold is 1.5V DC with 200mV of hysteresis.

For output control, 32 open-drain outputs are connected in tandem with 32 input buffers to each I/O channel. The outputs are the open drains of individual mosfets. The gates of the mosfets are driven by the FPGA. The sources of these mosfets are connected in common. This configuration provides up to 32 low-side switches for digital control. Writing a '1' to the output will turn the switch ON (closed-circuit), a '0' will turn it OFF (open-circuit). Since the input buffers are connected in tandem with the output mosfets, efficient loopback monitoring of the output state can be accomplished by reading the input channel registers.

With respect to output control, the 100KΩ input buffer resistors in combination with +4.7V voltage clamps will tend to increase the off-state drain current with increased drain voltage (up to 0.5mA at 60V). This is due to the fact that the input buffer circuitry and output mosfet drain circuitry are connected in tandem to the same I/O pin. If this presents a problem for your application, then you should consider separating the inputs and outputs by using other boards like the Acromag IP400 40-channel input board and the IP405 40-channel output board.

Output operation is considered 'Fail-safe'. That is, the outputs are always OFF upon power-up reset, and are automatically cleared following a system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions. Further, unlike some competitive units, output gate pulldowns are included to ensure that the outputs do not turn on momentarily when output load power is applied with no power to the IP module.

The output mosfets employed are rated for a much higher current than specified. However, the field connector and cabling used are only rated to 1A per pin (limiting a single channel to 1A). For compatibility with other IP models, 10 pins have been reserved for ground return (hence; the 10A total current limitation placed on this module). The low R_{dsON} of the output mosfets will ensure TTL-level compatible logic-low output signals even at high (1A) output currents.

The output mosfets include an integrated zener diode between the drain and the source. This provides output voltage clamp protection to 60V. The tandem input channel is also rated to 60V. However, when driving inductive loads such as relay coils, you should always place a shunt diode across the load to shunt the reverse EMF that develops across the coil when the current through it is turned off (refer to Section 2 and see Drawing 4501-520 for an example of this type of protection).

Since the input buffer and output mosfet circuitry share an I/O pin, inputs and outputs may be intermixed in any combination. Further, by providing an input channel for each output, efficient loopback monitoring of the output state can be easily accomplished (see Drawing 4501-522).

Digital input channels of this model can be configured to generate interrupts for Change-Of-State (COS) and input level (polarity) match conditions at selected input channels (channels 0-7 only). Interrupt service is prioritized with the higher numbered channels having higher priority over the lower numbered channels. An 8-bit interrupt service routine vector is provided during interrupt acknowledge cycles on data lines D0...D7. The interrupt release mechanism employed is RORA (Release On Register Access).

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). Not all of the IP logic P1 pin functions are used. P1 also provides +5V and +12V power to the module (-12V is not used).

All I/O, address decoding, control signals, interrupt handling, and ID access logic, is done through an FPGA installed on the IP module. It also returns the acknowledgement signal required by the carrier board per the IP specification. The program for the gate array is stored in separate PROM memory and loaded upon reset.

An ID PROM (read only) installed in the IP module provides the identification for the individual module per the IP specification. The ID PROM, input and interrupt registers are all accessed through the 16-bit data bus interface to the carrier board.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment. Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Operating Temperature.....0 to +70°C.
Relative Humidity.....5-95% Non-Condensing.
Storage Temperature.....-55°C to +125°C.
Physical Configuration.....Single Industrial I/O Pack Module.
  Length.....3.880 in. (98.5 mm).
  Width.....1.780 in. (45.2 mm).
  Board Thickness.....0.062 in. (1.59 mm).
  Max Component Height.....0.314 in. (7.97 mm).
Connectors:
  P1 (IP Logic Interface).....50-pin female receptacle header (AMP 173279-3 or equivalent).
  P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).
Power:
  +5 Volts (±5%).....13mA, Typical with outputs OFF; 28mA, Typical with outputs ON; 50mA Maximum.
  +12 Volts (±5%) from P1.....7.3mA Typical; 8.5mA Maximum.
  -12 Volts (±5%) from P1.....0mA (Not Used)
Non-Isolated.....Logic and field commons have a direct electrical connection.

DIGITAL INPUTS

Input Channel Configuration.....32 non-inverting buffered inputs with a common connection. For DC voltage applications only, observe proper polarity.
Input Signal Voltage Range.....0 to +60V DC, Maximum.
Input Signal Threshold.....TTL compatible. 1.5V DC with 200mV of hysteresis, typical. Thus, Low-to-High threshold is 1.6VDC, High-to-Low is 1.4VDC, typical. Limited to TTL levels of 0.8VDC (Max LOW level) and 2.0VDC (Min HIGH level).
Input Resistance.....100KΩ, Typical.
Input Hysteresis.....200mVDC centered at a 1.5VDC threshold, Typical.
Input Current.....560uA, Typical at 60VDC.
Interrupt Input Response Time.....250nS minimum to 375nS maximum, depending on when the input transition occurs with respect to the 8MHz clock. Measured from input transition to INTREQ0 line assertion.

DIGITAL OUTPUTS

Output Channel Configuration.....32 open-drain DMOS Mosfets with common source connection. For DC voltage applications only, observe proper polarity.

Output "OFF" Voltage Range.....0 to +60V DC, Maximum.

Output "OFF" Leakage Current.....25uA Maximum (Mosfet Only, 55°C, 48V). Does not include tandem input bias current. NOTE: The 100KΩ input buffer resistors in combination with +4.7V voltage clamps will tend to increase the off-state drain current with increased drain voltage (up to 0.5mA at 60V). This is due to the fact that the input buffer circuitry and output mosfet drain circuitry are connected in tandem to the same I/O pin.

Output "ON" Current Range.....0 to +1A DC, continuous (up to 10A total for all channels combined), or 300mA DC, continuous (all channels ON). No deration required at elevated ambients.

Output R_{ds} ON Resistance.....0.2Ω, Maximum (25°C).

Turn-ON Time.....Varies with load, 320ns Typical, with 330Ω pull-up to +5V and 12-inch ribbon cable. Measured from IOSEL line assertion to output drain state transfer to TTL 0.8V level.

Turn-OFF Time.....Varies with load, 500ns Typical, with 330Ω pull-up to +5V and 12-inch ribbon cable. Measured from IOSEL line assertion to output drain state transfer to TTL 2.0V level.

Resistance to RFI.....No digital upsets occur for field strengths up to 10V per meter at 27MHz, 151MHz, & 460MHz per SAMA PMC 33.1 test procedures.

Resistance to EMI.....Unit has been tested with no digital upsets under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Withstand Capability.....Outputs exhibit no damage when tested with a standardized test waveform representative of surges (high frequency transient electrical interference) per ANSI/IEEE C37.90-1978.

ESD Protection.....Outputs exhibit no degradation of performance with repeated ESD induced voltages to ± 6KV per DOD-STD-1686.

OUTPUT MOSFETS

(These specifications are included for reference and apply to the output driver only. See DIGITAL OUTPUTS above for module specifications).

Manufacturer/Part Number.....National NDS9945, Siliconix Si9945DY.

Voltage V_{DSS}.....60V DC, Maximum.

Current I_D.....3.5A, Continuous (25°C), 2.8A, Continuous (70°C).

ON Resistance R_{DS}.....0.2Ω (VGS=4.5V, 25°C).

Power Dissipation P_D.....2W (25°C).

Output "OFF" Leakage Current....25uA Maximum (55°C, 48V).

INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per revision 0.7.1.

Electrical/Mechanical Interface.....Single-Size IP Module.

IP Data Transfer Cycle Types Supported:

- Input/Output (IOSel*).....16-bit word (D16), or 8-bit even or odd byte (D08(EO)) data Read/ Write on D0...D15.
- ID Read (IDSel*).....32 x 8 ID PROM read on D0..D7.

Access Times (8MHz Clock):

- ID PROM Read.....1 wait state (375ns cycle).
- Channel Register Read.....1 wait state (375ns cycle).
- Channel Register Write.....1 wait state (375ns cycle).
- Interrupt Registers Read.....1 wait state (375ns cycle).
- Interrupt Registers Write.....1 wait state (375ns cycle).

Interrupts:

- Handling Format.....An 8-bit vector is provided during interrupt acknowledge cycles on D0...D7. The release mechanism is RORA type (Release On Register Access).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

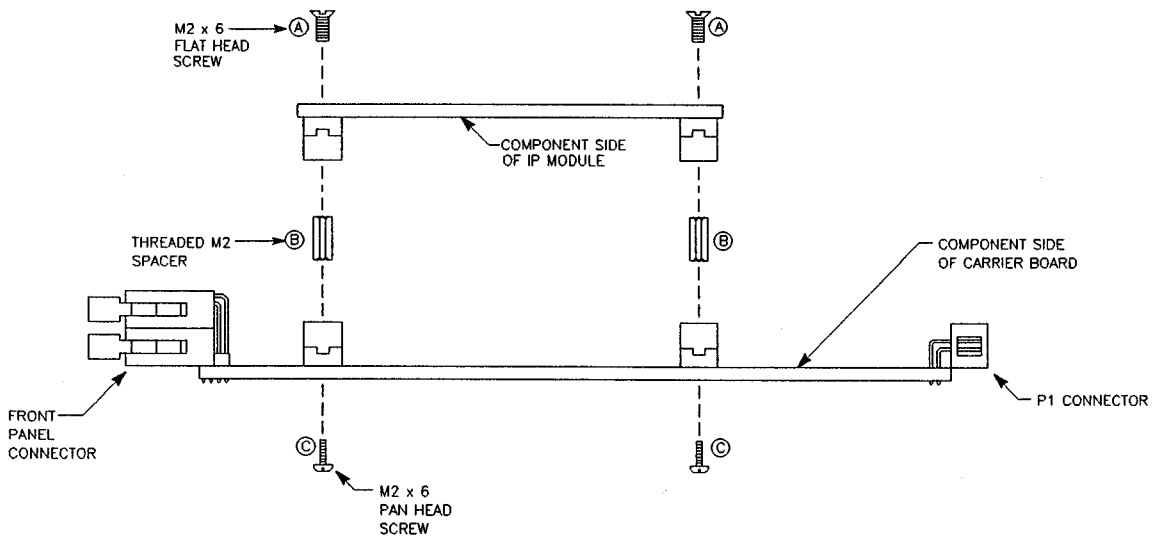
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.



ASSEMBLY PROCEDURE:

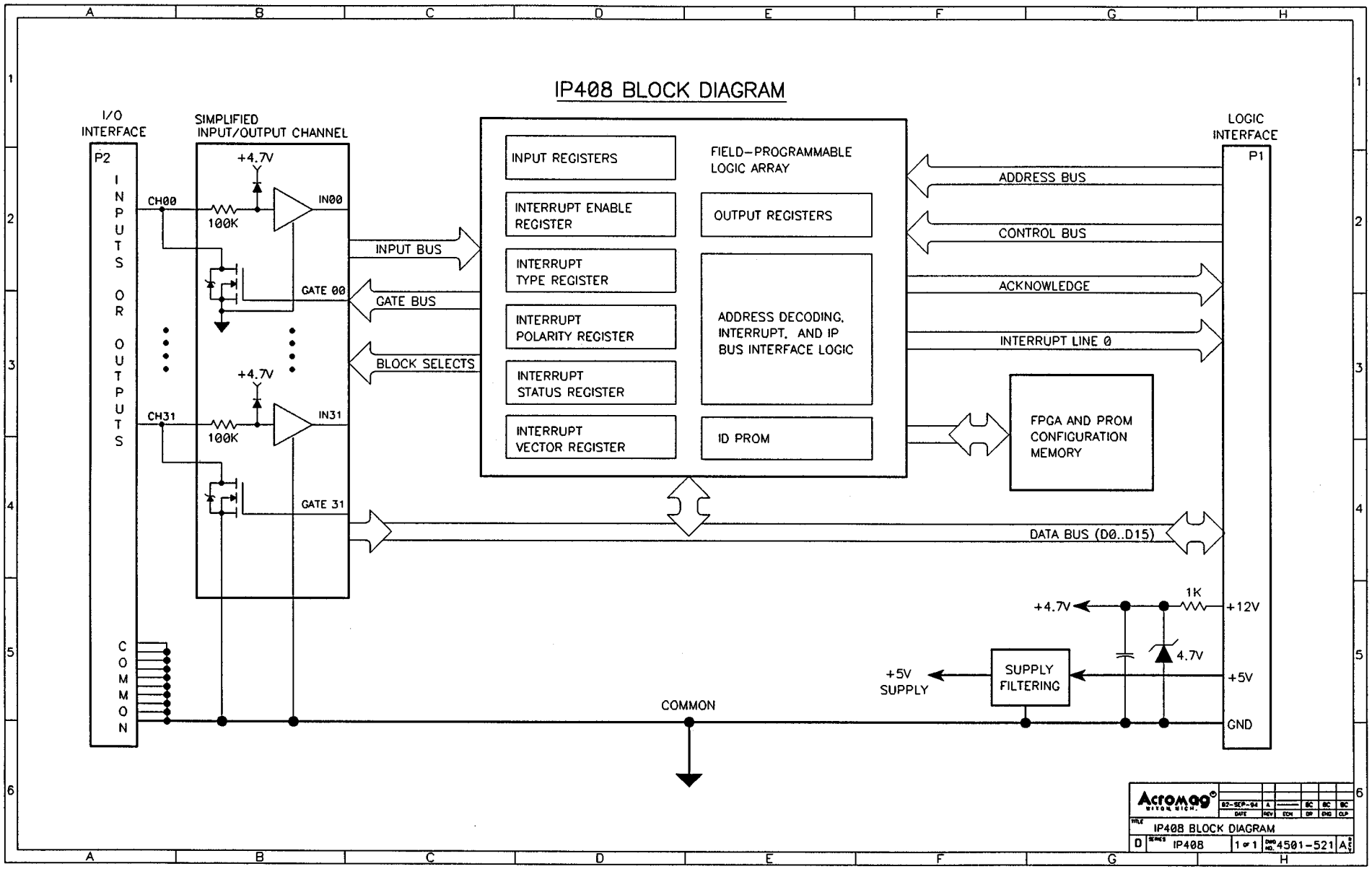
1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

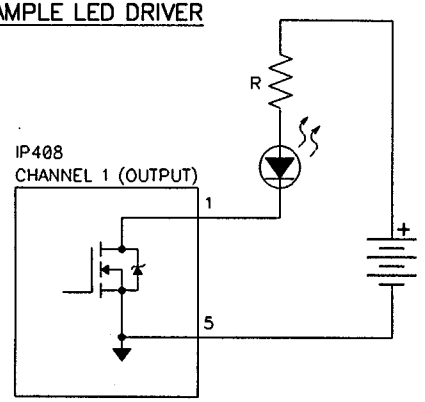
Acromag WIXOM, MICH.						
29 JUL 94	B	94C911	TAV	JGV	BC
21 DEC 93	A	——	TAV	JGV	BC
DATE	REV	ECN	DR	ENG	CLP

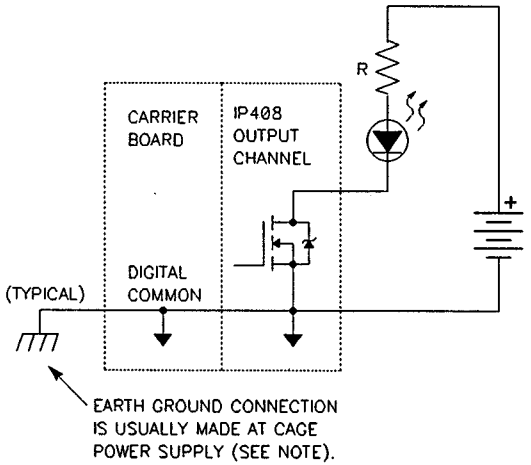
TITLE: IP MECHANICAL ASSEMBLY

SIZE	SERIES		DWG NO.	REV
D	IP	1 of 1	4501-434	B

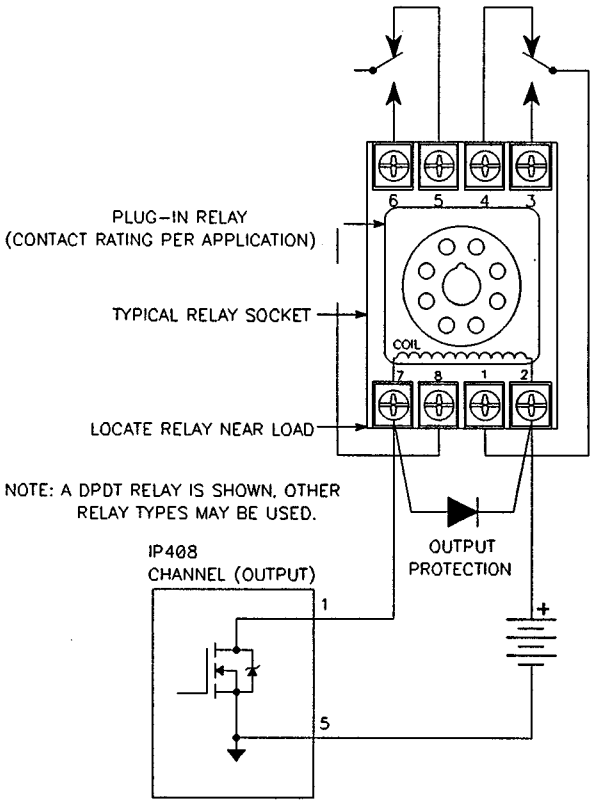

IP408 BLOCK DIAGRAM
I/O INTERFACE
SIMPLIFIED INPUT/OUTPUT CHANNEL
LOGIC INTERFACE
P2
INPUTS OR OUTPUTS
COMMON
CH00
CH31
100K
+4.7V
IN00
IN31
GATE 00
GATE 31
INPUT BUS
GATE BUS
BLOCK SELECTS
INPUT REGISTERS
INTERRUPT ENABLE REGISTER
INTERRUPT TYPE REGISTER
INTERRUPT POLARITY REGISTER
INTERRUPT STATUS REGISTER
INTERRUPT VECTOR REGISTER
FIELD-PROGRAMMABLE LOGIC ARRAY
OUTPUT REGISTERS
ADDRESS DECODING, INTERRUPT, AND IP BUS INTERFACE LOGIC
ID PROM
FPGA AND PROM CONFIGURATION MEMORY
P1
ADDRESS BUS
CONTROL BUS
ACKNOWLEDGE
INTERRUPT LINE 0
DATA BUS (D0..D15)
1K
+12V
4.7V
+5V
GND
+5V SUPPLY
SUPPLY FILTERING
COMMON
Acromag
IP408 BLOCK DIAGRAM
IP408
4501-521

EXAMPLE LED DRIVER

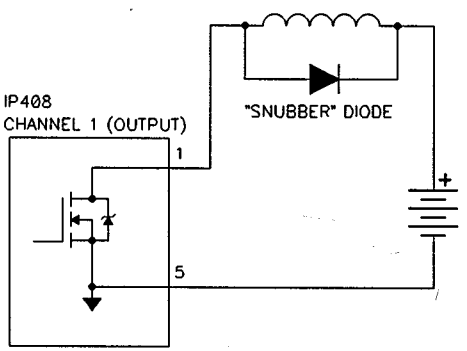




CONNECTION TO AN INTERPOSING RELAY FOR GREATER DRIVE CAPABILITY

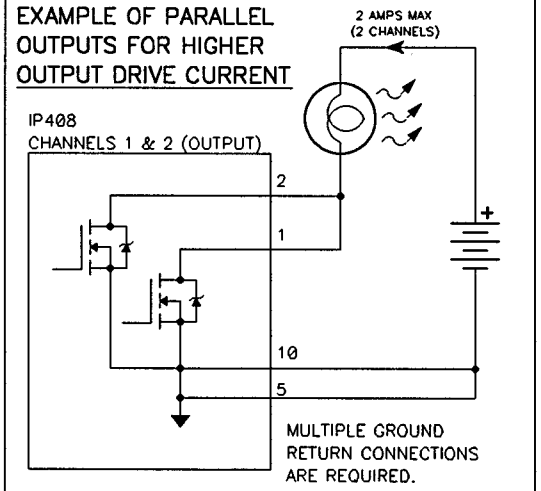


EXAMPLE RELAY/COIL DRIVER



NOTE: THE "SNUBBER" DIODE IS USED TO SHUNT THE REVERSE EMF THAT DEVELOPS WHEN THE CURRENT THROUGH THE COIL IS TURNED OFF. THIS WILL HELP PROLONG THE LIFE OF THE OUTPUT CHANNEL.

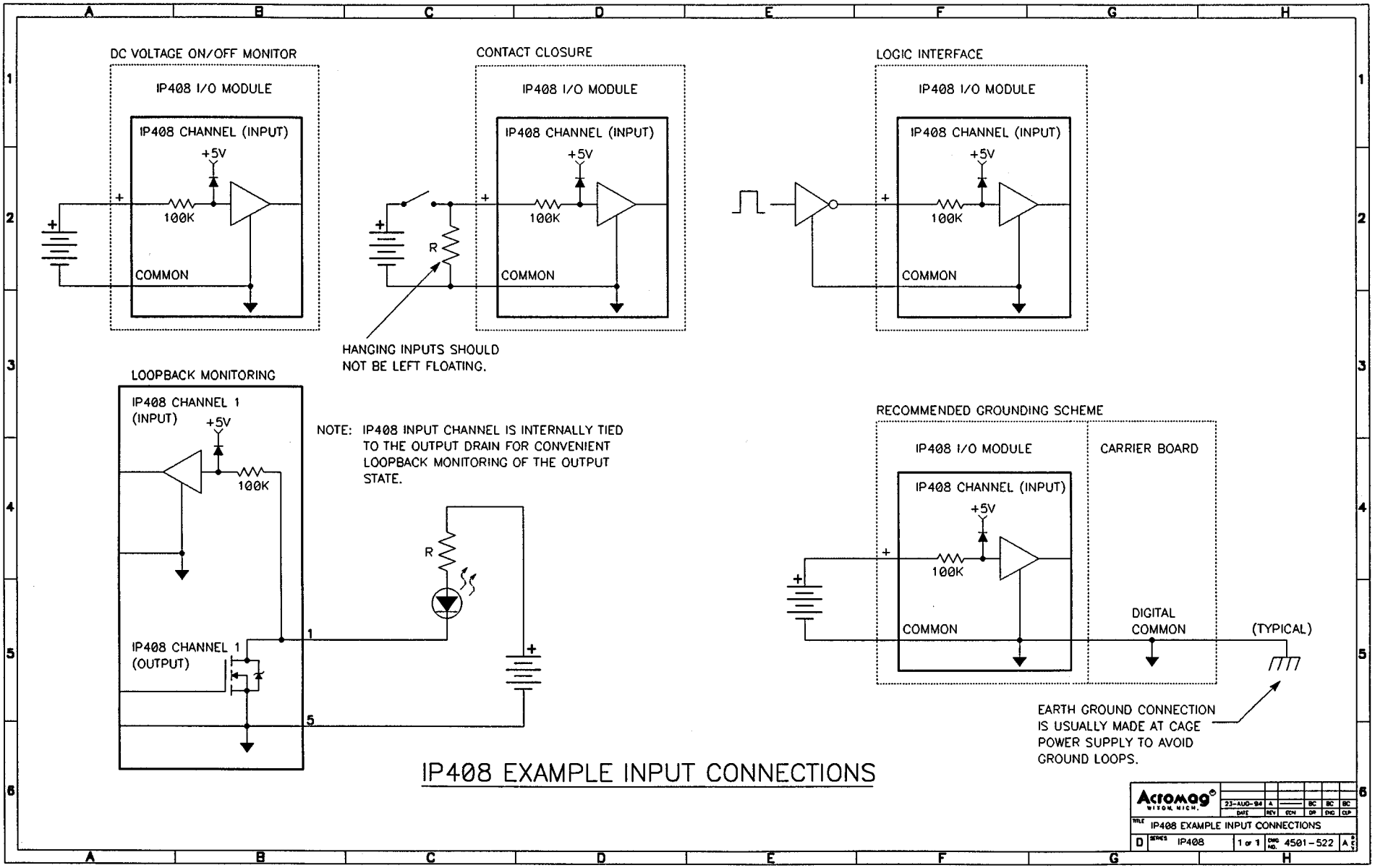
EXAMPLE OF PARALLEL OUTPUTS FOR HIGHER OUTPUT DRIVE CURRENT



NOTE: MULTIPLE EARTH GROUNDS CAUSE GROUND LOOPS AND MUST BE AVOIDED.

IP408 EXAMPLE OUTPUT CONNECTIONS

Acromag							
	23-AUG-94	A		BC	BC	BC
	DATE	REV	ECN	DR	ENG	CUP
TITLE: IP408 EXAMPLE OUTPUT CONNECTIONS							
D	SERIES: IP408	1 of 1	DWG NO. 4501-520	A			



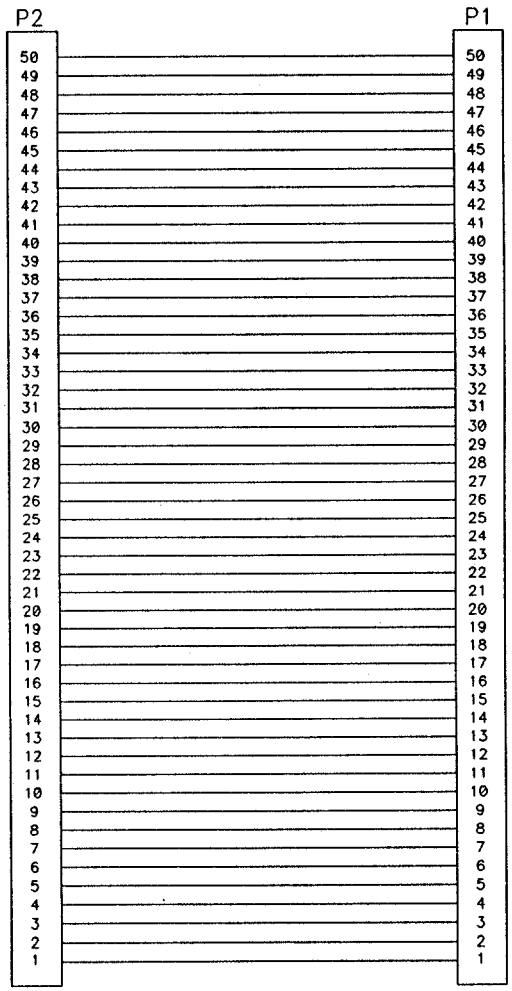
IP408 EXAMPLE INPUT CONNECTIONS

Acromag WIXOM, MICH.

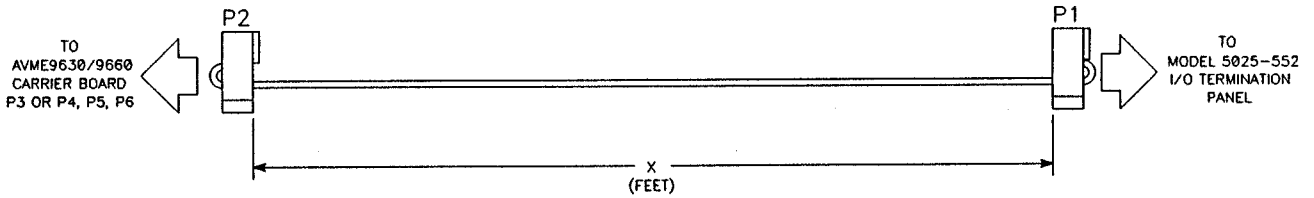
DATE	REV	ECN	DR	ENG	CLP
23-AUG-04	A		BC	BC	BC

TITLE: IP408 EXAMPLE INPUT CONNECTIONS

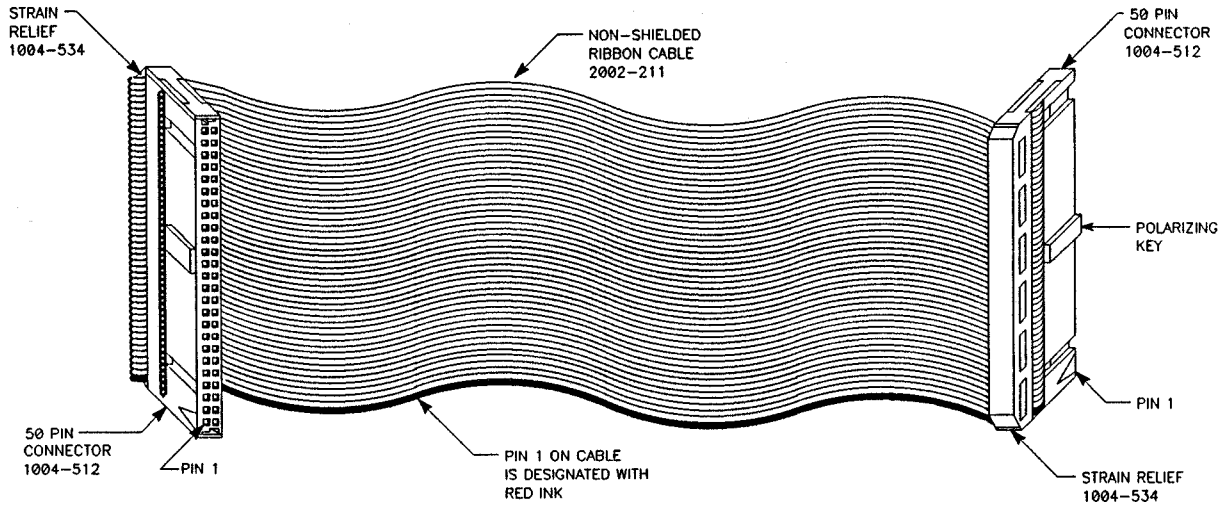
D | SERIES: IP408 | 1 of 1 | DWG NO. 4501-522 | A



MODEL 5025-550-x SCHEMATIC



TOP VIEW

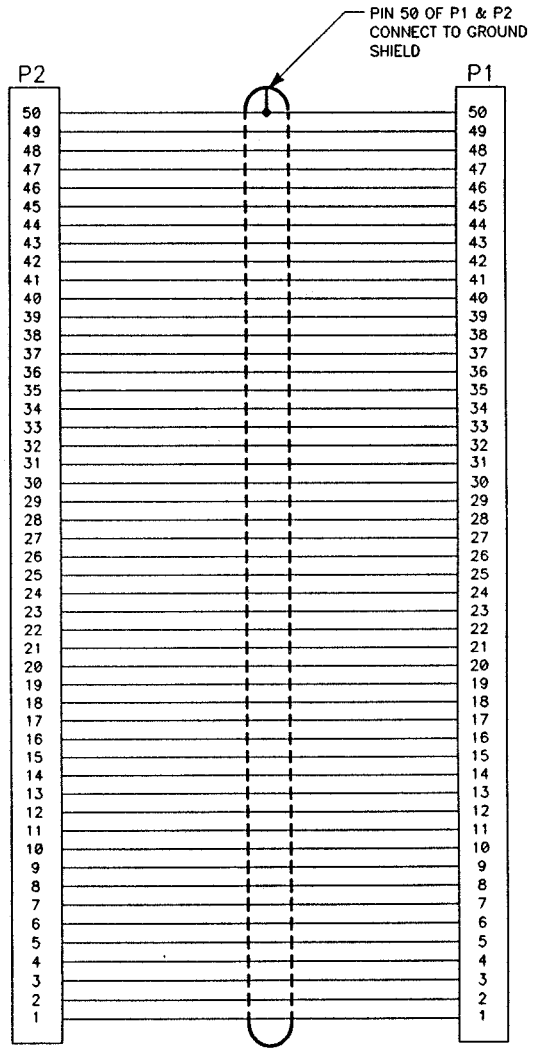


FRONT VIEW

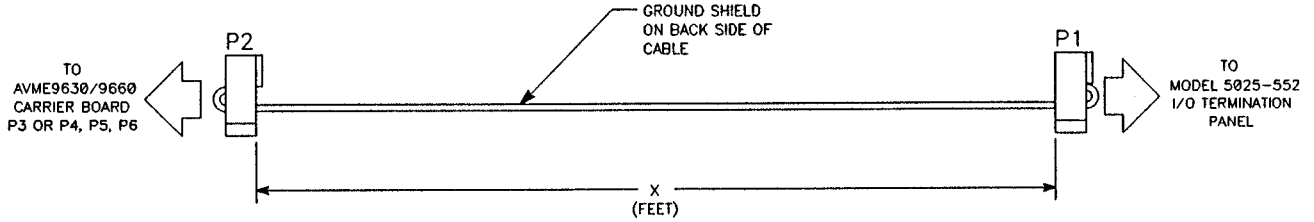
NOTE: SEVEN DIGIT PART NUMBERS ARE
ACROMAG PART NUMBERS (XXXX-XXX).

MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

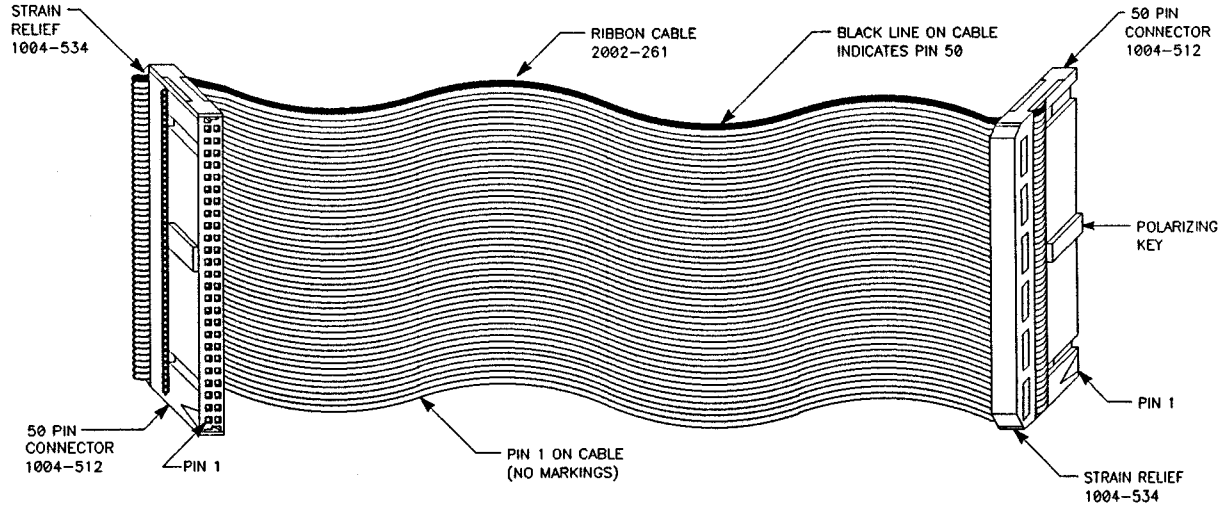
Acromag WIXOM, MICH.
09 FEB 94 A
DATE REV ECN DR ENG CLP
TITLE CABLE 5025-550-x, NON-SHIELDED
D SERIES 1 OF 1 DWG NO. 4501-462 A



MODEL 5025-551-x SCHEMATIC



TOP VIEW

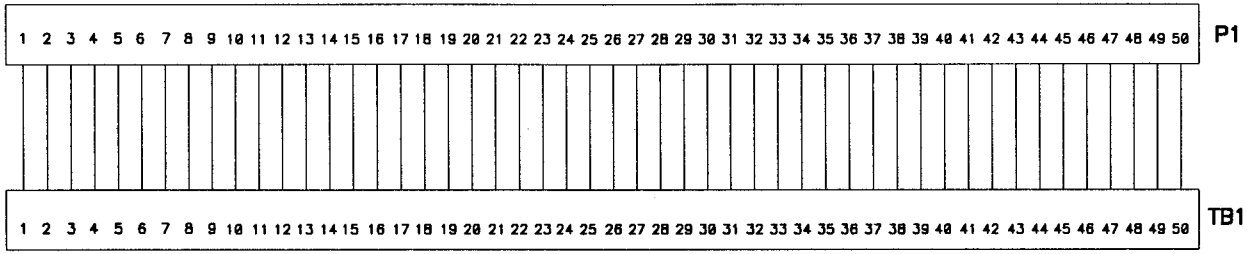


FRONT VIEW

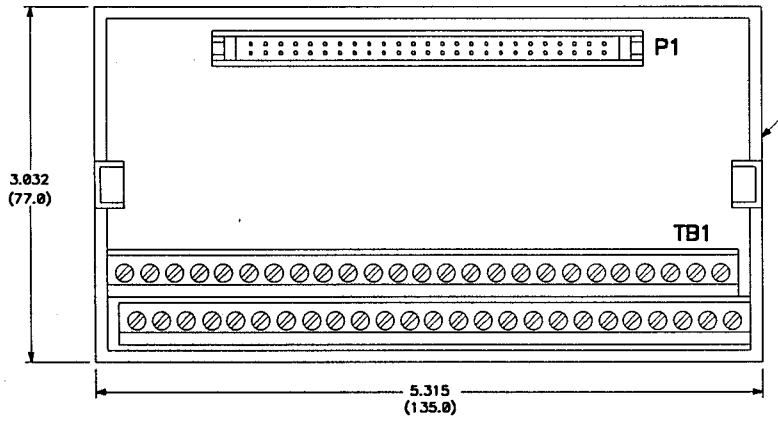
NOTE: SEVEN DIGIT PART NUMBERS ARE
ACROMAG PART NUMBERS (XXXX-XXX).

MODEL 5025-551-x SIGNAL CABLE, SHIELDED

Acromag WIXOM, MICH.
95 FEB 94 | A | — | T&V | CAP | BC
DATE | REV | ECN | DR | CHG | CLP
TITLE: CABLE 5025-551-x, SHIELDED
D | SERIES | 1 OF 1 | DWG NO. 4501-463 | A

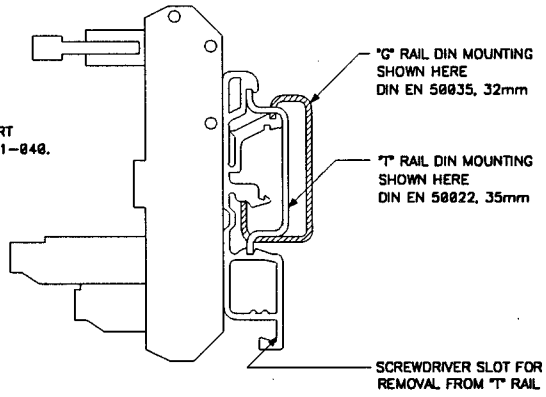


MODEL 5025-552 TERMINATION PANEL SCHEMATIC

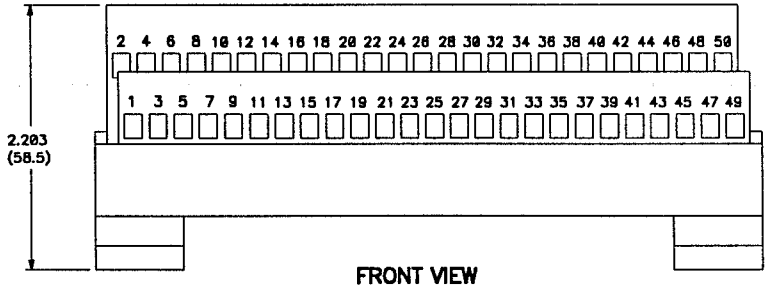


TOP VIEW

TERMINATION PANEL ACROMAG PART NUMBER 4001-040.



SIDE VIEW



FRONT VIEW

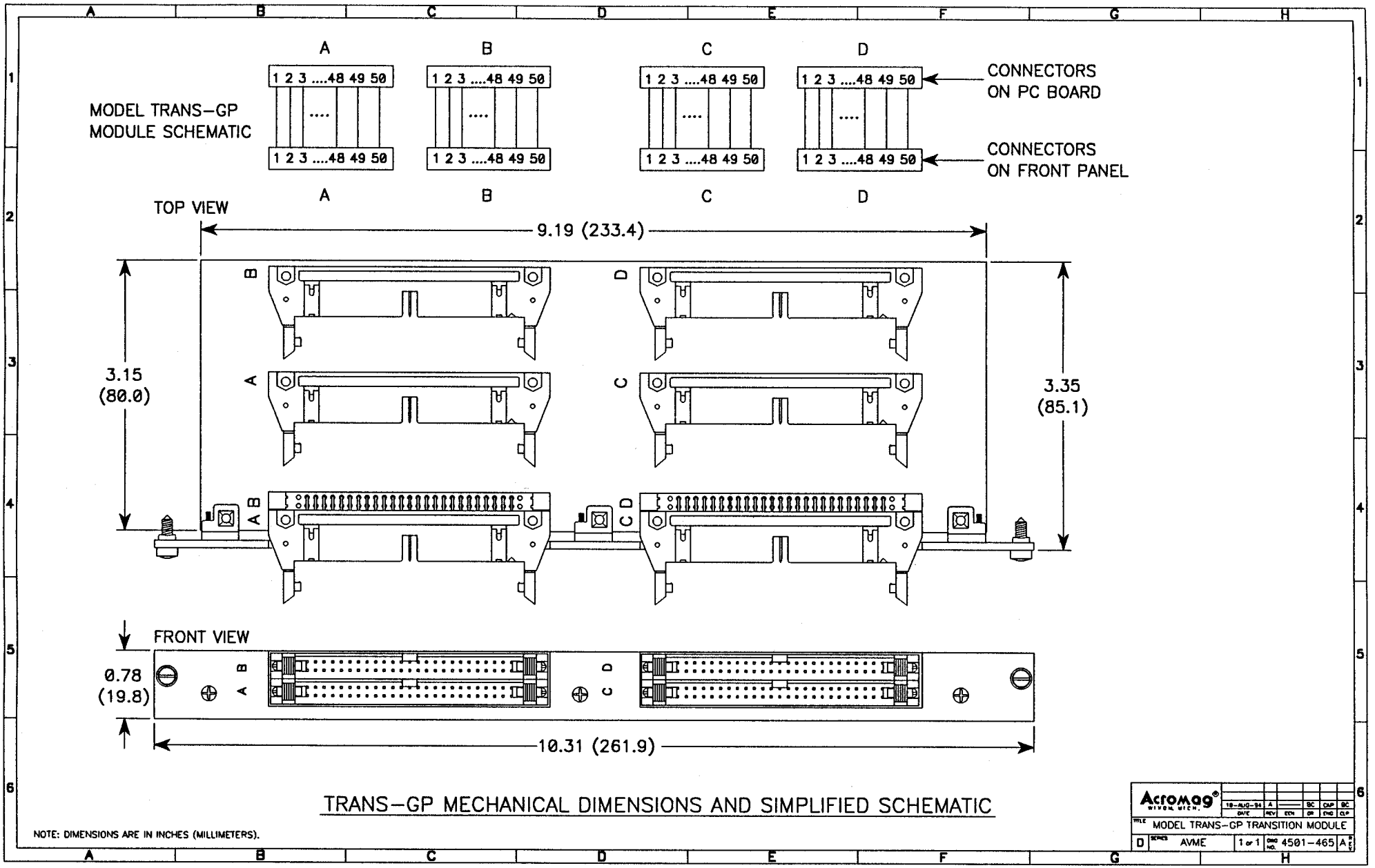
NOTES:

DIMENSIONS ARE IN INCHES (MILLIMETERS).

TOLERANCE: ±0.020 (±0.5).

MODEL 5025-552 TERMINATION PANEL

Acromag® WIXOM, MICH.						
	09 FEB 94	A	—	TAV	CAP	BC
	DATE	REV	ECN	DR	ENG	CLP
TITLE: MODEL 5025-552 TERMINATION PANEL						
D SERIES	1 OF 1	DWG NO. 4501-464		A REV		



TRANS–GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

Acromag® WIXOM, MICH.

DATE	REV	ECN	DR	ENG	CLP
18-AUG-94	A	——	BC	CAP	BC

TITLE: MODEL TRANS–GP TRANSITION MODULE

D | SERIES: AVME | 1 of 1 | DWG NO. 4501–465 | A REV