SIS3302
1510 Firmware - Gamma

Addendum
to
User Manual
V1408

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Revision Table:

Revision	Date	Modification
1.32	04.12.09	**Design Version: 1408** - change Fir Trigger Filter • reduced maximum Peaking time and Gap time values to 511 clocks • expanded decimation: 1/2/4/8/16 • add Trigger Extended Threshold registers
Xxx Addendum	10.11.2010	**Design Version: 1510** - remove MCA Mode - add "Raw data Wrap Mode " • raw data sample length up to 65532 • additional pretrigger delay up to "raw data sample length" - 4 - add FIR-CFD Trigger (75%,50%) - maximum Internal Gate Length expanded from 63 clocks to 255 clocks - maximum Internal Trigger Delay expanded from 63 clocks to 255 clocks

1 Table of contents

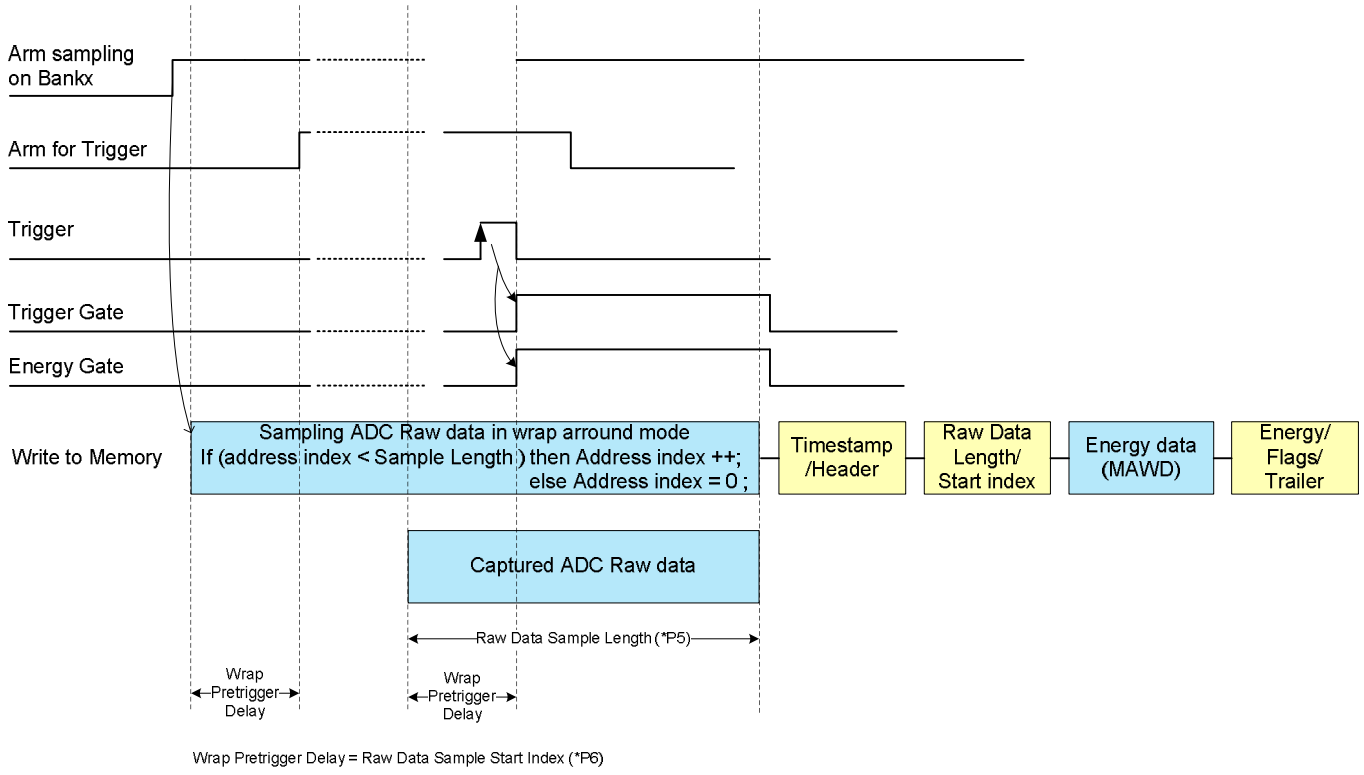
2 Modifications/Add-Ons

2.1 Raw Data Wrap Mode

A new set of registers are implemented to enable the “Raw Data Wrap Mode”.
If this mode is enabled then it is possible to capture up to (“Raw Data Sample Length” – 4) (Wrap Pretrigger Delay) samples priori to the trigger.

2.1.1 Application flow

The sampling of the raw data starts immediately with the Key-Cmd “Arm sampling on Bank X” and with each “end of event” in the memory space of the next “Event memory space”.
After “Wrap Pretrigger Delay” samples are written into the memory the logic will be armed for a trigger.
If a trigger occurs the logic writes “Raw Data Sample Length” – “Wrap Pretrigger Delay” into the memory in a wrap around mode and stops the Raw Data sampling.



2.1.2 Register

One new register is added (Raw Data Buffer Control Mode) and the meaning/function of one register will change if the “RawDataBufferControlWrapMode” bit is set.

2.1.2.1 Raw Data Buffer Control Mode registers

```
#define SIS3302_RAW_DATA_BUFFER_CONTROL_MODE_ALL_ADC        0x0100002C

#define SIS3302_RAW_DATA_BUFFER_CONTROL_MODE_ADC12          0x0200002C
#define SIS3302_RAW_DATA_BUFFER_CONTROL_MODE_ADC34          0x0280002C
#define SIS3302_RAW_DATA_BUFFER_CONTROL_MODE_ADC56          0x0300002C
#define SIS3302_RAW_DATA_BUFFER_CONTROL_MODE_ADC78          0x0380002C
```

Bit	31	30-0
Function	RawDataBufferControlWrapMode	**reserved**

default after Reset: 0x0

RawDataBufferControlWrapMode = 1: Raw Data Sample Wrap Mode is enabled

2.1.2.2 Raw Data Buffer Configuration registers

```
#define SIS3302_RAW_DATA_BUFFER_CONFIG_ALL_ADC         0x0100000C

#define SIS3302_RAW_DATA_BUFFER_CONFIG_ADC12           0x0200000C
#define SIS3302_RAW_DATA_BUFFER_CONFIG_ADC34           0x0280000C
#define SIS3302_RAW_DATA_BUFFER_CONFIG_ADC56           0x0300000C
#define SIS3302_RAW_DATA_BUFFER_CONFIG_ADC78           0x0380000C
```

The meaning/function will change if the RawDataBufferControlWrapMode bit is set.

RawDataBufferControlWrapMode = 0 (old meaning/function)

Bit	Function
31	Bit 15 of Raw Data Sample Length
…	…
18	Bit 2 of Raw Data Sample Length
17	0 (quad sample aligned values only)
16	0 (quad sample aligned values only)
15	Bit 15 of Raw Data Sample Start Index
…	…
1	Bit 1 of Raw Data Sample Start Index
0	0 (even values only)

RawDataBufferControlWrapMode = 1 (new meaning/function)

Bit	Function
31	Bit 15 of Raw Data Sample Length
…	…
18	Bit 2 of Raw Data Sample Length
17	0 (quad sample aligned values only)
16	0 (quad sample aligned values only)
15	Bit 15 of **Wrap Pretrigger Delay**
…	…
1	Bit 1 of **Wrap Pretrigger Delay**
0	0 (even values only)

Both values are 16-bit deep. The number of samples has to be quad sample aligned and the number of Wrap Pretrigger samples has to be even.

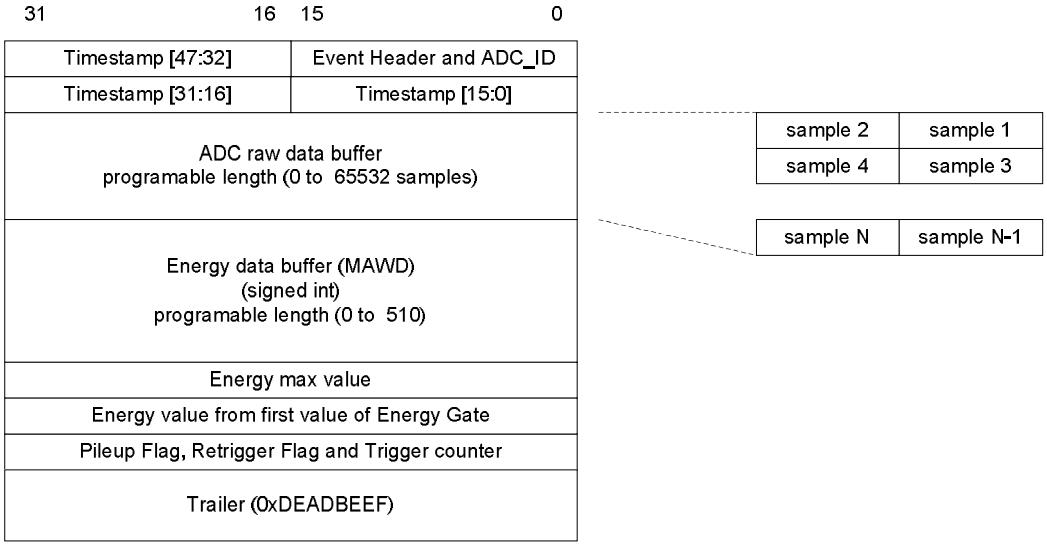
The number of “Raw Data Sample Length” is limited to 65532 samples!
The number of “Wrap Pretrigger Delay” is limited to (“Raw Data Sample Length” – 4)!

Note: The Trigger Gate Length has to be greater than
(“Raw Data Sample Length” - “Wrap Pretrigger Delay”) but max. to 0xffff.
See “calculate_energy_trigger_windows_and_parameters (void)” in
sis3302_configuration.c

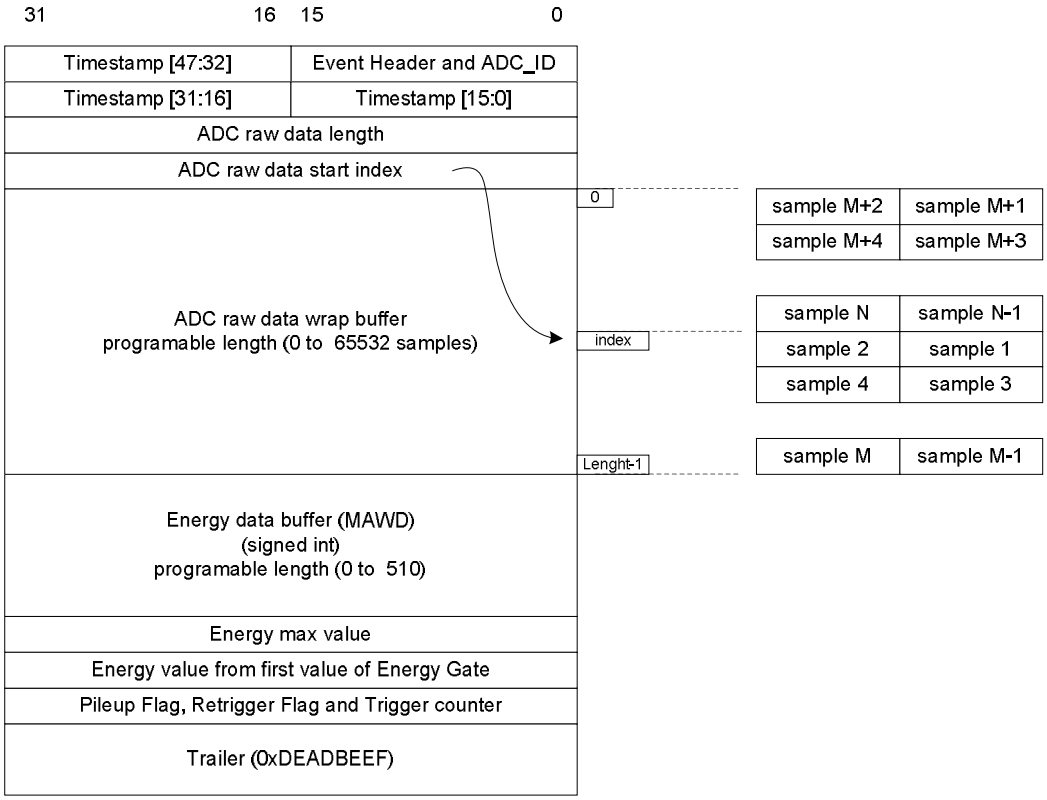
2.1.3 Event Buffer Data Format

The Event Data Format will change if the “RawDataBufferControlWrapMode” bit is set.

RawDataBufferControlWrapMode = 0 (old meaning/function)



RawDataBufferControlWrapMode = 1 (new meaning/function)



Two 32-bit words are added to the Event Buffer: “ADC raw data length" and “ADC raw data start index“.

Raw Data Rearange Example :

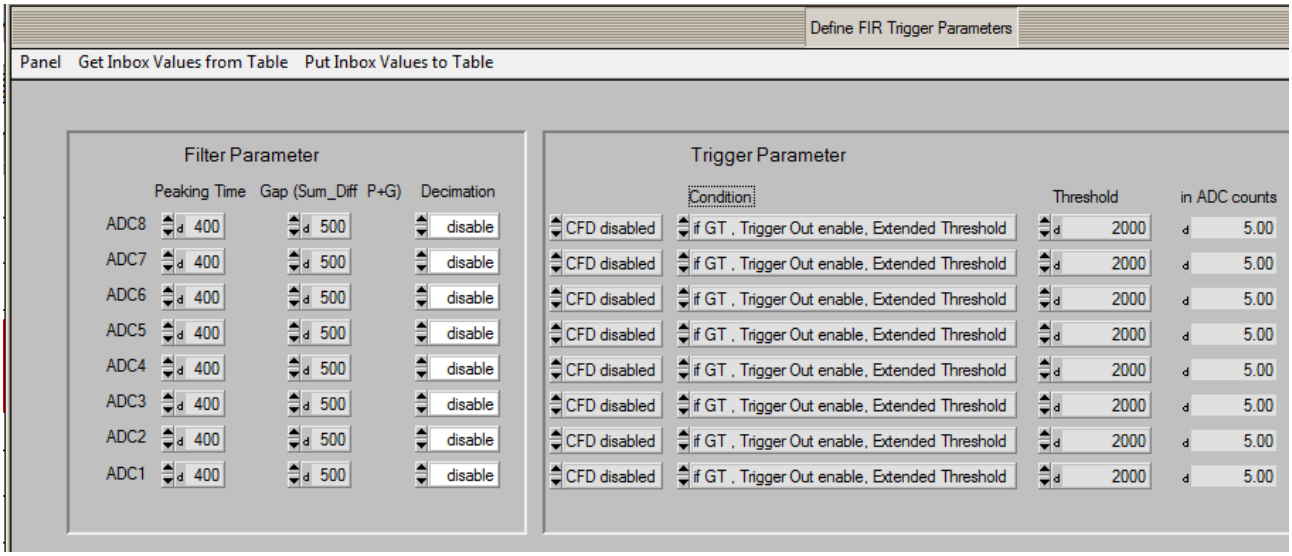
```
int displayEventAdcRawData(unsigned int plot_size, unsigned int* buffer_ptr, int plot_color)
{
 int check_on ;
 unsigned short ushort_temp ;
 unsigned short* ushort_buffer_ptr ;
 unsigned int i,j;
 unsigned int nof_wrap_samples, wrap_start_index;

 if (plot_size > 0) {

    if (gl_uint_RawDataWrapModeFlag != 0) {
        nof_wrap_samples =  buffer_ptr[0] ;
        wrap_start_index =  buffer_ptr[1] ;

        j=wrap_start_index;
        ushort_buffer_ptr = (unsigned short*) (buffer_ptr+2) ;

        for (i=0;i<nof_wrap_samples;i++) {
            gl_short_raw_data_wrap_buffer[i] =  ushort_buffer_ptr[j] ;
            j++;
            if(j >= nof_wrap_samples ) {j=0;}
        }

        PlotY (Panels[PANEL_DISPLAY_RAW], PANEL_RAW_GRAPH_RAW, gl_short_raw_data_wrap_buffer,
                    plot_size,  VAL_UNSIGNED_SHORT_INTEGER, gl_plot_raw_plot_style,
                    VAL_NO_POINT, gl_plot_raw_line_style, 1, plot_color);

    }
    else { // (gl_uint_RawDataWrapModeFlag == 0)
        PlotY (Panels[PANEL_DISPLAY_RAW], PANEL_RAW_GRAPH_RAW, (unsigned short*) buffer_ptr,
                  plot_size,  VAL_UNSIGNED_SHORT_INTEGER, gl_plot_raw_plot_style, VAL_NO_POINT,
                  gl_plot_raw_line_style, 1, plot_color);
    }
 }
return 0;
}
```

Call in sis3302_gamma_running.c:

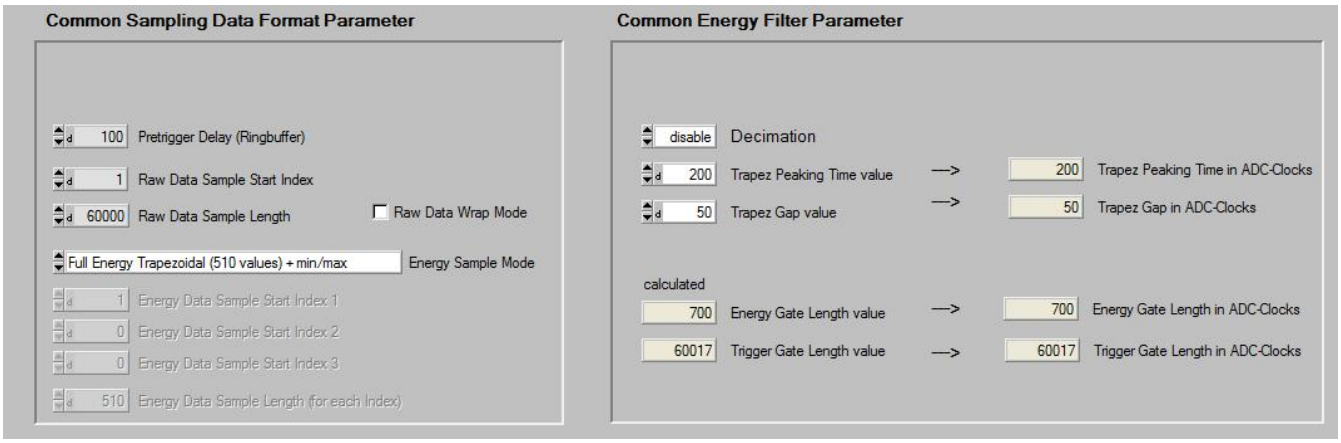
```
displayEventAdcRawData((gl_uint_RawSampleLength),
                        &gl_dma_rd_buffer[event_index_offset + raw_data_index],
                        raw_plot_color[channel_index])     ;
```

2.1.4 CVI Examples

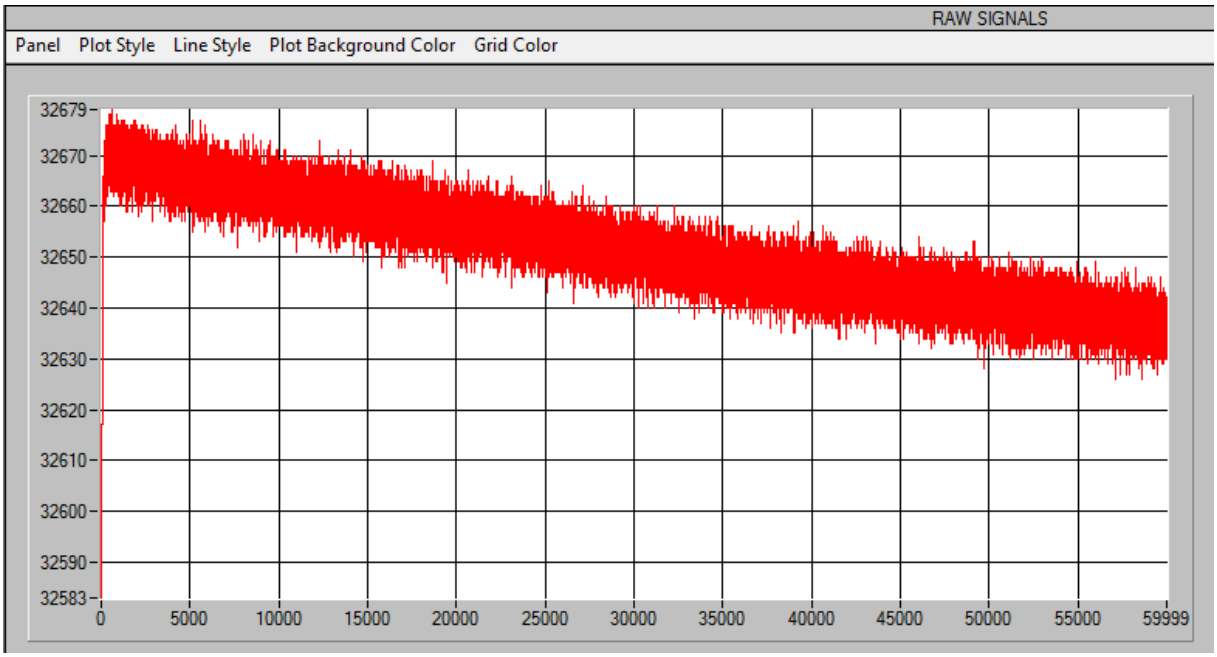
2.1.4.1 Trigger parameter



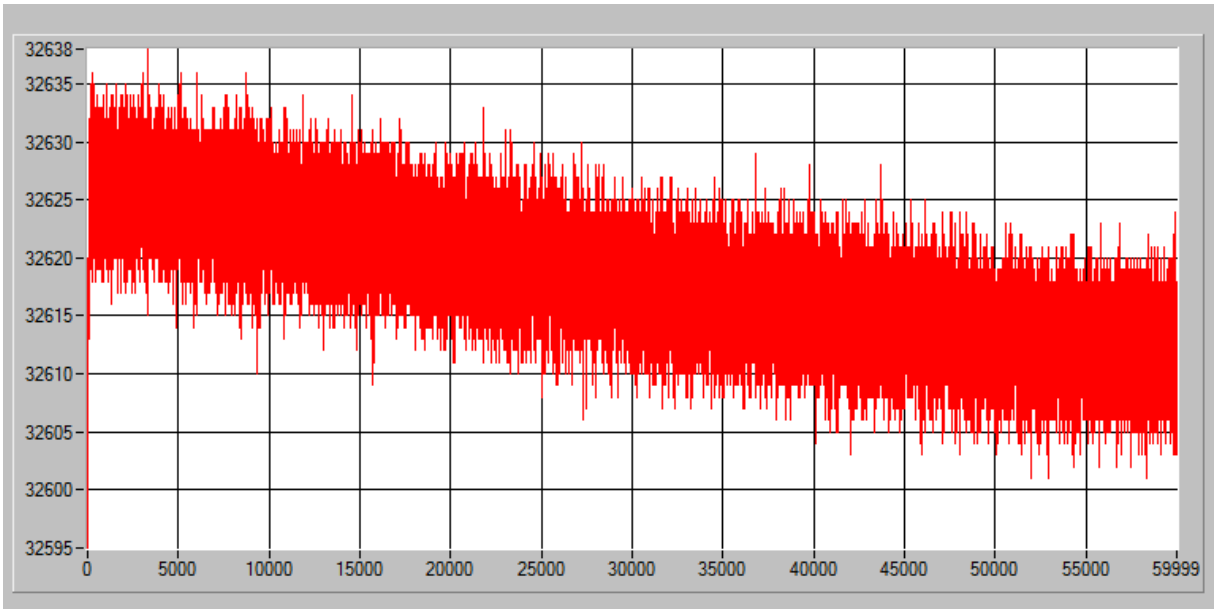
2.1.4.2 Sampling Parameter with Wrap Mode = 0



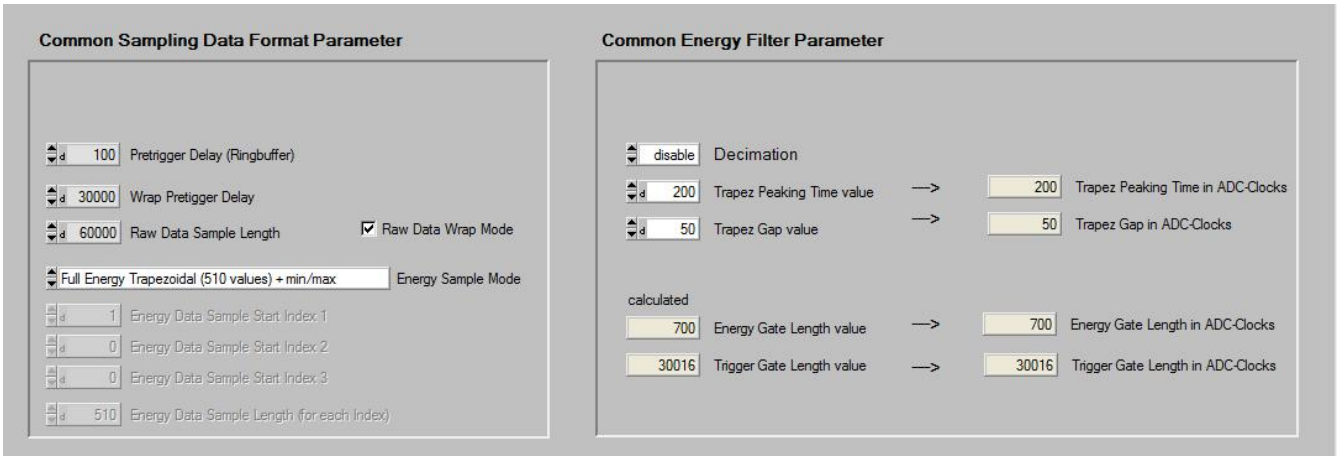
2.1.4.3 Plot of 6mV signal with Wrap Mode = 0



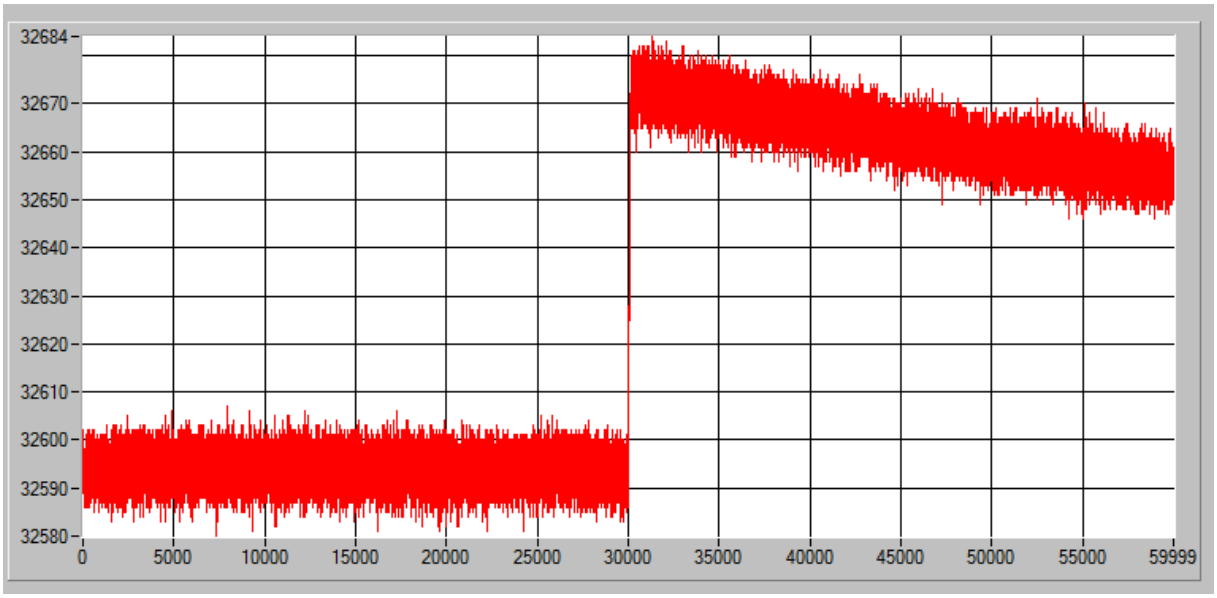
2.1.4.4 Plot of 2mV signal with Wrap Mode = 0



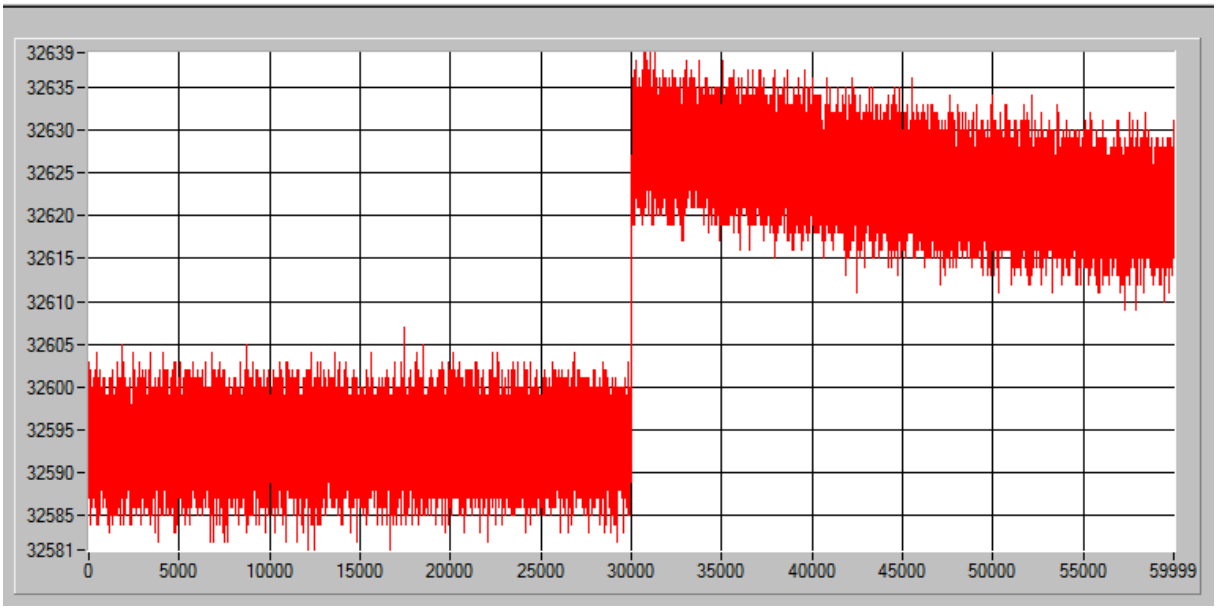
2.1.4.5 Sampling Parameter with Wrap Mode = 1



2.1.4.6 Plot of 6mV signal with Wrap Mode = 1



2.1.4.7 Plot of 2mV signal with Wrap Mode = 1



2.2 FIR CFD Trigger

Two new CFD control bits are added to the “Trigger Threshold” register.

2.2.1 Trigger Threshold registers

```
#define SIS3302_TRIGGER_THRESHOLD_ADC1          0x02000034
..
#define SIS3302_TRIGGER_THRESHOLD_ADC8          0x0380003C
```

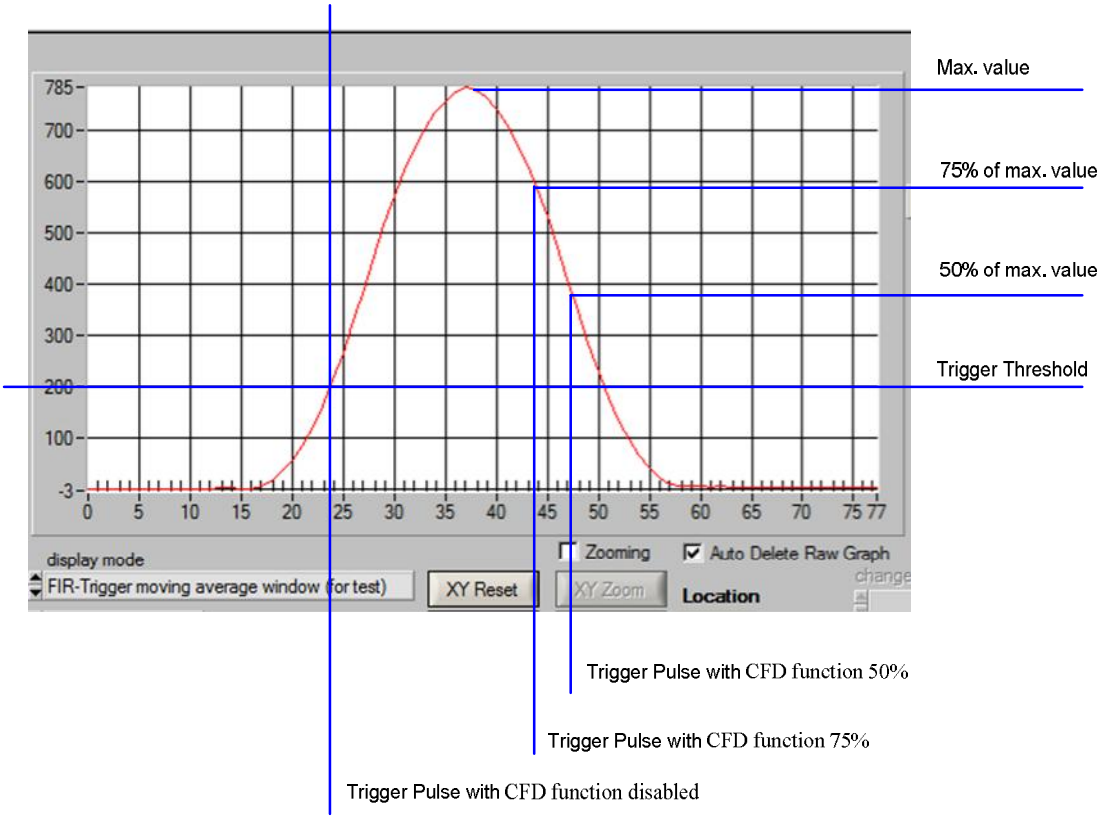
Bit	31-27	26	25	24	23	22	21-20	19-17	16-0
Function	none	Disable Trigger Out	Trigger Mode GT	none	Extended Threshold Mode	none	**CFD control bits**	none	**Trapezoidal** threshold value

default after Reset: 0x0

CFD control bit setting table:

CFD Control Bit 1	CFD Control Bit 0	CFD function
0	0	CFD function disabled
0	1	CFD function disabled
1	0	CFD function enabled with 75%
1	1	CFD function enabled with 50%

P = 10, G = 10 (sumG = 20)
Signal rise time 100ns

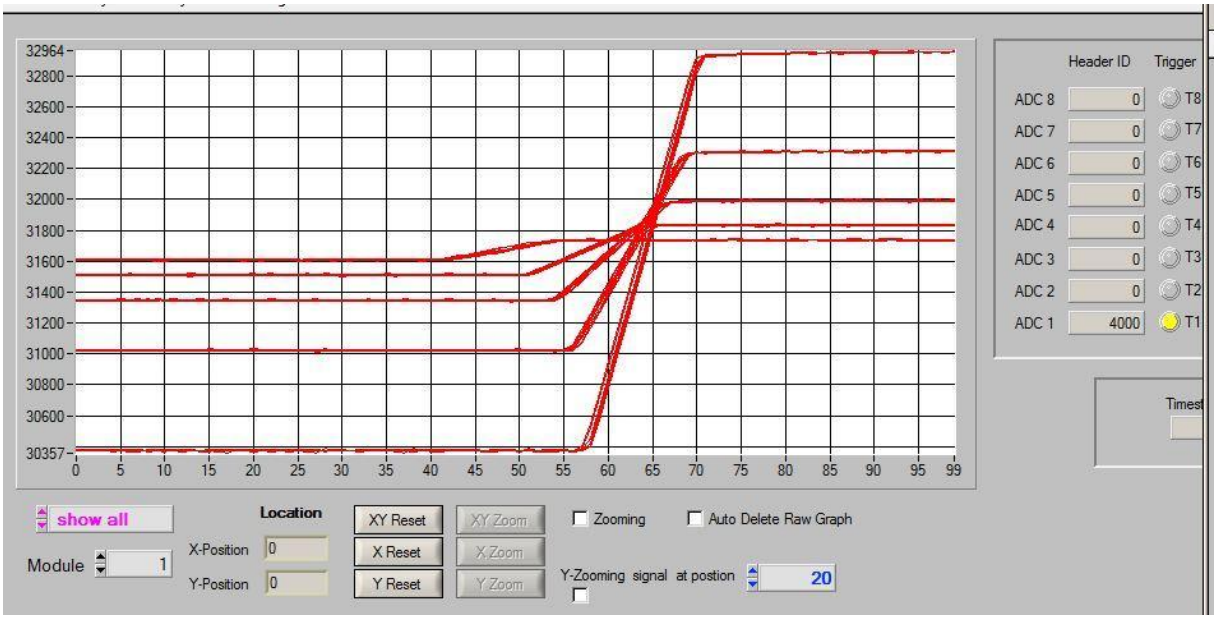


2.2.2 CVI Examples

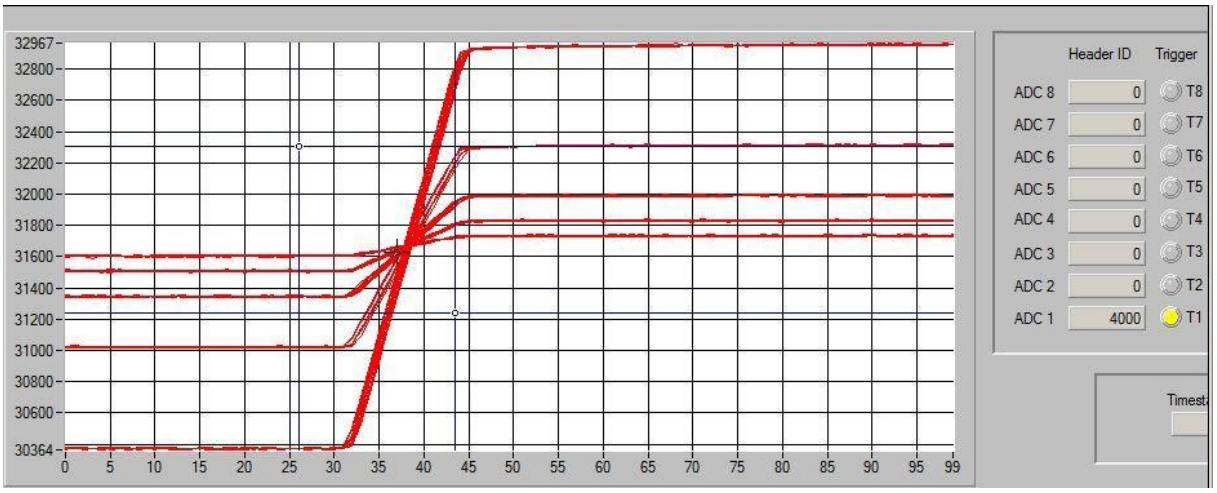
Signal rise time: 100ns
Signal amplitude:10mV, 25mV, 50mV, 100mV and 200mV

The plots show 10 events of each amplitude

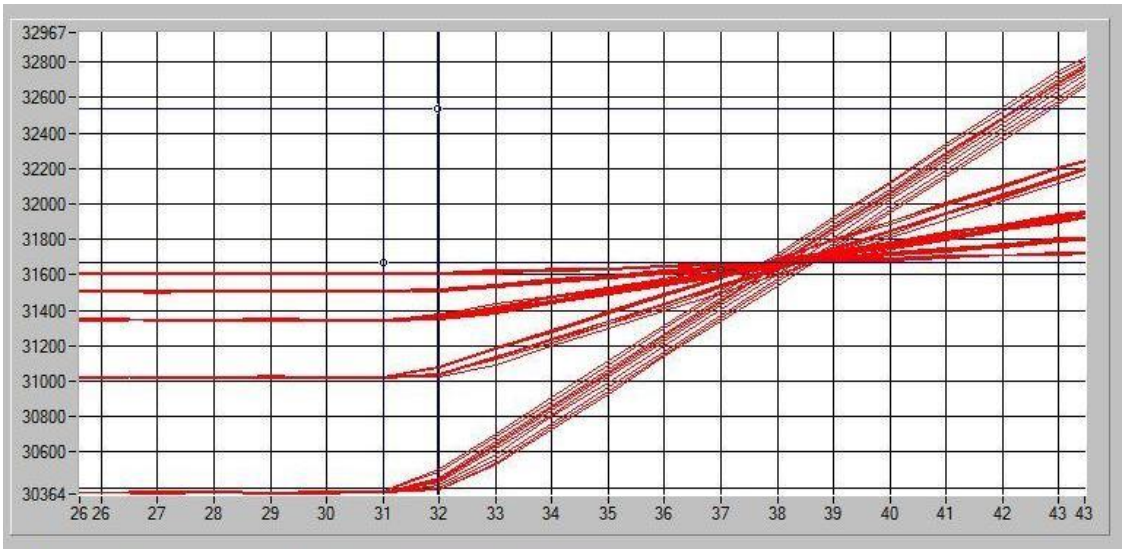
2.2.2.1 Plot of Raw data with CFD disabled



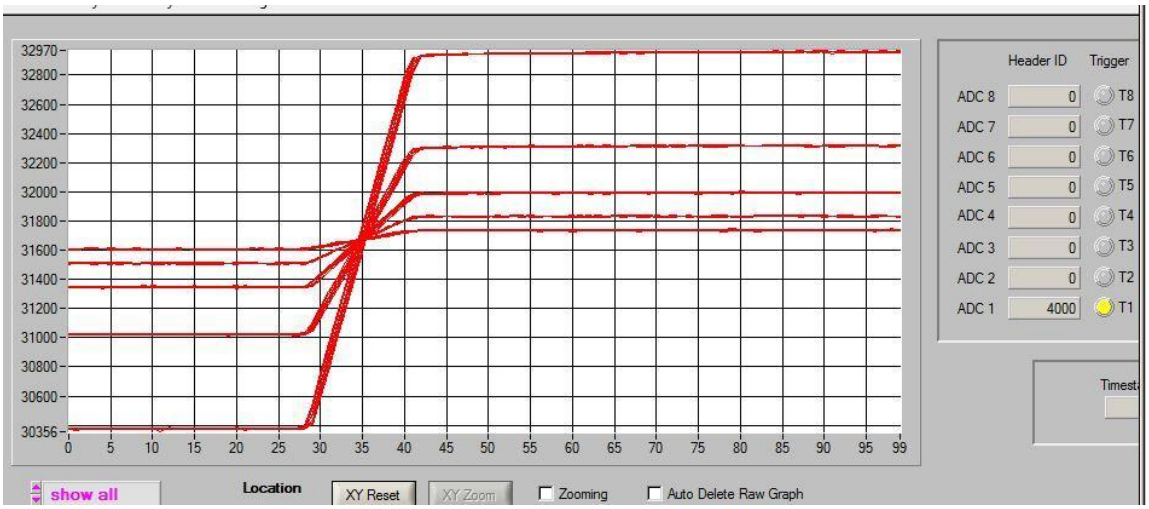
2.2.2.2 Plot of Raw data with CFD 75% enabled



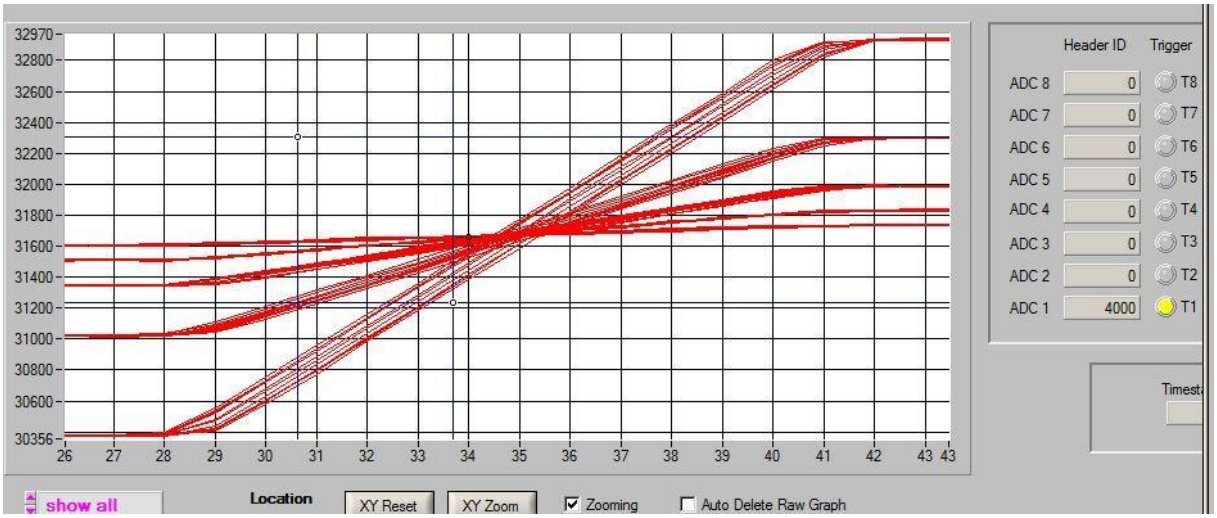
2.2.2.3 Plot of Raw data with CFD 75% enabled zoomed



2.2.2.4 Plot of Raw data with CFD 50% enabled



2.2.2.5 Plot of Raw data with CFD 50% enabled zoomed



3 Programming Hints

3.1 ADC Clock source

Do not use the “first” internal 100 MHz (Acquisition Control register, Clock Source bits = 000). Use instead of the “second” internal 100MHz (Clock Source bits = 111) .

3.2 Disarm Sample Logic and ARM sampling on Bank x

After “Disarm” or “Disarm and Arm on Bank x” you have to wait or to check if the sampling is disabled or if the sampling Bank is swapped.
After “Disarm” it could be that the last event is still sampling and the logic waits to disarm/swap the bank until the last event is written.

After disarm: wait for a time (max. 100us) which one Event needs to copy to the memory.

After disarm and arm on other Bank:

```
if (bank1_armed_flag == 1) {
   addr = gl_uint_SIS3302_BroadcastAddrConf + SIS3302_KEY_DISARM_AND_ARM_BANK2 ;
   bank1_armed_flag = 0; // bank 2 is armed
}
else {
   addr = gl_uint_SIS3302_BroadcastAddrConf + SIS3302_KEY_DISARM_AND_ARM_BANK1 ;
   bank1_armed_flag = 1; // bank 2 is armed
}


//read Acquisition register to check if Bank is swapped (old Bank busy with last event ?)
poll_counter = 0 ;
addr = gl_uint_ModAddrRun[module_index] + SIS3302_ACQUISITION_CONTROL ;
poll_loop_valid = 1;
do {
   sub_vme_A32D32_read(addr,&data_rd );
   poll_counter++;
   if (bank1_armed_flag == 1) { // Bank1 is armed and Bank2 (page 4) has to be readout
       if ((data_rd & 0x10000) == 0x10000)  { poll_loop_valid = 0; } // is swapped
   }
   else {
       if ((data_rd & 0x20000) == 0x20000)  { poll_loop_valid = 0; } // is swapped
   }

   if (poll_counter > 500) { // max length = eventlength (raw samples * 10ns) + energy Length
                             // max= 100us
        poll_loop_valid = 0;
   }
} while (poll_loop_valid==1)  ;
```

Now the logic swapped to the other bank and the value of the register “previous_bank_sample_address_reg” is valid.

3.3 Increase the VME BusError Time

Increase the VME BusError Time to 10us or higher on the VME Master/System Controller.

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