NCD GTID / Clock Card

M. Howe, J.L. Orrell, T. Van Wechel, J.F. Wilkerson

November 14, 2002

1 Design Specifications (Provided by T. Van Wechel)

The NCD GTID card provides the timing interface between the NCD data acquisition electronics and the SNO Trigger System[1]. The NCD GTID card communicates with the Master Trigger Card/Digital (MTC/D) which is part of the SNO Trigger System.

The MTC/D card receives trigger signals from several sources including the NCD GTID card, analyses the trigger inputs and determines when a valid event has occurred and generates a global trigger signal. Each global trigger increments the 24 bit global ID trigger counter consisting of a Lower 16 bit counter and an Upper 8 bit counter. The MTC/D card also has a 42 bit 50MHz counter and a 52 bit 10MHz counter. The 50MHz and 10MHz count at each global trigger along with the global trigger count are recorded to provide time information for each valid event. Each front end card in the SNO system as well as the NCD GTID card has a global trigger ID counter that is synchronized with the MTC/D global trigger counter. This synchronization is provided over the time bus. The time bus has 4 signals, GTRIG which increments the GTID counter by one count, SYCNLR which resets the Lower 16 bit counter, SYNCLR24 which resets the Upper 8 bit counter and PED (Pedestal) which is used for calibrations of the SNO system but not for the NCD system.

The NCD GTID card also has a local VME clock counter that can be used for timing when the SNO MTC/D is not available. The VME clock counter is a 48 bit counter that counts the 16MHz VME clock and is optionally recorded with each valid NCD event. The NCD GTID card accepts NCD MUX events from the NCD trigger output from the NCD MUX controller card. Also NCD shaper events are accepted from the daisy chained enable/disable outputs from the NCD shaper cards. The correlation of NCD MUX and Shaper events in hardware and or software still needs additional development.

2 Register Definitions (Provided by T. Van Wechel)

For the prototype NCD GTID board the Base address is 7000 and the AM is 29 or 2D.

READ COMMANDS

- Read Board ID Register. Address=Base + 10
  - BID<7..0> = Board ID (board serial #), BID<10..8> = Board Type (0=test, 1=emiT, 2=NCD,3=timetag, 4=emiTclock, 5=GTID), BID<15..11> = Board Revision.(The GTID board is presently at Revision 2 to update to new BID register definition).
- Read Status Register, Address=Base+12.
  - STATUS REGISTER<0>= NCD Mux Event.
  - STATUS REGISTER<1>= NCD Shaper ADC Event.
  - STATUS REGISTER<2> = Valid NCD GT Clock (This means that a Global Trigger pulse has been received after a valid NCD Event and that the GTID register and VME clock registers may be read).

[1] The SNO Trigger System, University of Pennsylvania, October 12, 1997.

- STATUS REGISTER<3> = Count Error (This occurs if at a SYNCLR, the Lower GTID count is not equal to FFFF. This is to test if the local GTID counter is out of sync with the MTC/D GTID count.)
- STATUS REGISTER<4> = VME Clock Counter Enabled. (This is a status bit to indicate that the VME clock counter has been enabled.)

- Read Lower GTID Register. Address = Base + 14.
  - LOWER GTID REGISTER<15..0> = GTID_REG<15..0>.
- Read Upper GTID Register. Address = Base + 16.
  - UPPER GTID REGISTER<7..0> = GTID_REG<23..16>.
- Read Lower VME Clock Counter Register. Address = Base + 18.
  - LOWER VME CLOCK COUNT REGISTER<15..0> = VME_CLK_CNT_REG<15..0>.
- Read Middle VME Clock Counter Register. Address = Base + 1A.
  - MIDDLE VME CLOCK COUNT REGISTER<15..0> = VME_CLK_CNT_REG<31..16>.
- Read Upper VME Clock Counter Register. Address = Base + 1C.
  - MIDDLE VME CLOCK COUNT REGISTER<15..0> = VME_CLK_CNT_REG<47..32>.

WRITE COMMANDS

- Register Reset. Address = Base + 00.
  - Resets most internal registers in the Altera Chip. The VME Clock Counter, the VME Clock Counter Registers, the GTID Registers, the NCD Mux Event, NCD Shaper ADC Event and the Valid NCD GT Clock status bits the VME Clock Counter Enable and the Multiboard Output Enable register are reset by the Register Reset Command. The GTID counter is NOT reset by this command. (After using the GTID board we may realize that some of the registers that are reset by this command should not be.)
- Fast Clear. Address = Base + 02.
  - This is a holdover command from the shaper boards. It has no function at the present time.
- NCD GT Event Reset. Address = Base + 08.
  - This command clears the NCD Mux Event, NCD Shaper ADC Event and the Valid NCD GT Clock status bits. This command should be used after the Global Trigger pulse associated with an event has occurred and reading the GTID registers and optionally the VME Clock Count Registers
- Multiboard Output Enable. Address = Base + 0A. D<0> = 1 Enables, D<0> = 0 Disables.
  - This command enables the Multiboard I/O enable/disable inputs and outputs. The multiboard enable/disable input tells the GTID board that there has been an NCD Shaper ADC event. Must be enabled to have Shaper ADC events.
- VME Clock Counter Enable. Address = Base + 0C. D<0> = 1 Enables, D<0> = 0 Disables.
  - Turns the VME Clock Counter On or Off.
- VME Clock Counter Reset. Address = Base + 0E.
  - Resets the VME Clock Counter to zero.

- Load Lower GTID Counter. Address = Base + 14.
  - Loads D<15..0> into GTID<15..0>.
- Load Upper GTID Counter. Address = Base + 16.
  - Loads D<8..0> into GTID<23..16>.
- Load Lower VME Clock Counter. Address = Base + 18.
  - Loads D<15..0> into VME_CLK_CNT<15..0>.
- Load Middle VME Clock Counter. Address = Base + 1A.
  - Loads D<15..0> into VME_CLK_CNT<31..16>.
- Load Upper VME Clock Counter. Address = Base + 1C.
  - Loads D<15..0> into VME_CLK_CNT<47..32>.

****

The following instructions should not be used during a run using the MTC/D card or the GTID board will become out of sync with the MTC/D.

- Software GTRIG. Address = Base + 20.
  - Simulates a GTRIG (Global Trigger) pulse on the time bus. Increments the GTID Counter by one count.
- Software SYNCLR. Address = Base + 22.
  - Simulates a SYNCLR (Sync Clear) pulse on the time bus. Resets the Lower GTID Counter to 0000.
- Software GTRIG AND SYNCLR. Address = Base + 24.
  - Simulates a simultaneous GTRIG and SYNCLR on the time bus. The specifications for the GTID Counter[2] say that the counter is incremented on the rising edge of GTRIG and is latched on the trailing edge of GTRIG. At rollover, on the next GTRIG following the count of FFFE, the counter increments to FFFF, than a SYNCLR pules is output sometime during the GTRIG pulse resetting the counter to 0000, so that 0000 is latched into the GTID register at the end of the GTRIG pulse. Also at the leading edge of the SYNCLR pulse there is a check to see that the GTID count is equal to FFFF. If not the Count Error Status bit is set.
- Software SYNCLR24. Address = Base + 26.
  - Simulates a SYNCLR24 pulse on the time bus. Resets the Upper GTID counter to 00.
- Test Latch GTID Register. Address = Base + 28.
  - Latches the current GTID count into the GTID register. If this instruction is used during a valid NCD event it may latch an invalid count into the GTID register.
- Test Latch VME Clock Count Register. Address = Base + 2A.
  - Latches current VME Clock count into the VME Clock Count Register. If this instruction is used during a valid NCD event the count loaded into the VME Clock Count register will be wrong for that event.

[2]The SNO Trigger System, University of Pennsylvania, October 12, 1997, page 46.

2.1 Suggested Command Sequence for a NCD event.

1. Poll the GTID Card with the Read Status Register command until the NCD Mux Event and/or ADC Shaper Event status bits are set. Eventually there will be more logic to correlate Mux and ADC Shaper events if they are close enough in time, but this still needs to be defined better.

2. If the MTC/D card is being used a GTRIG pulse should be issued on the time bus. If the MTC/D card is not in use than a Software GTRIG should be issued.

3. After the GTRIG (hardware or software) the Valid NCD GT Clock status bit is set, which is verified by using the Read Status Register command.

4. Now read the GTID register, by using the Read Lower GTID Register and Read Upper GTID Register commands. It is probably not necessary to read the Upper GTID register for every single event, as its count increments only once per 64K counts of the GTID.

5. If the MTC/D card is not in use the VME Clock Count register is also read now by using the Read Lower VME Clock Counter Register, Read Middle Clock Counter Register, and Read Upper VME Clock Counter Register commands. Since the Upper VME Clock counter only increments every 268.4 seconds it may not be necessary to read it for every event.

6. Use the NCD GT Event Reset command to clear the NCD Mux Event and/or ADC Shaper Event and the Valid NCD GT Clock status bits.

7. Return to step 1.

3 Software Status and Testing

Mark Howe has provided a NCD Trigger Card module for SHaRC with a Basic Ops window. John Orrell has tested the GTID / Clock Card.

To use the Bit3 617 VME Controller for low level tests one must have:

- Address Modifier: 29
- Address Space: Remote IO

The following features were tested using the NCD Trigger Card Basic Ops dialog and in most cases confirmed using the Bit3 617 VME Controller.

- "7000 ↕ Go" - What does this do?
- Slot x: What does this do? It appears to be required to be in "slot 4" to work.
- Board ID: Returns correct values: ID 40, TYPE 5, Rev 2.
- Status Register:
  - Single MUX input pulse: The MUX Event status register is correctly set. Tested on both VME controler and SHaRC's NCD Trigger module.
  - Enable Clock (and Disable) correctly reported.
  - Error Count only lasts for one read. This seems like strange behavior.
  - Valid GT Clock appears to work using a MUX input pulse followed by a Soft GT.
- Reset Register: Does not reset status register. Resets clock. Does not reset GTID counter. Does not reset Error Count bit in the status register.
- GTID Register: Button mislabeled. Is labeled "NCD GT Event Reset", should be labeled "Trigger Status Reset" or "Status Register Reset". This does correctly reset the NCD MUX Event, NCD ShaperADC (assumed actually), Valid NCD GT Clock.

- Reset Clock: Works.
- Read Lower, Middle, Upper Clock: Works.
- Load Lower, Middle, Upper Clock: Works.
- Read/Load GTID: Works.
- Soft GT: Appears to work - increments Lover GTID.
- SyncClr+SyncClr24: Works.
- Latch GTID: Works.
- Latch Clock: Works.
- GT/SyncClr: Lower GTID gets cleard and the Upper GTID gets incremented. That is, it works.

4 To-Do and Wish List

A more complete document. We need to add a higher level operations dialog to the NCD Trigger Card module. This dialog should provide a dummy data taking routine that “waits” for data and reads out GTID and clock information to the status window. From that dialog the associated methods can be used by the real data taking module in the NCD SHaRC system.

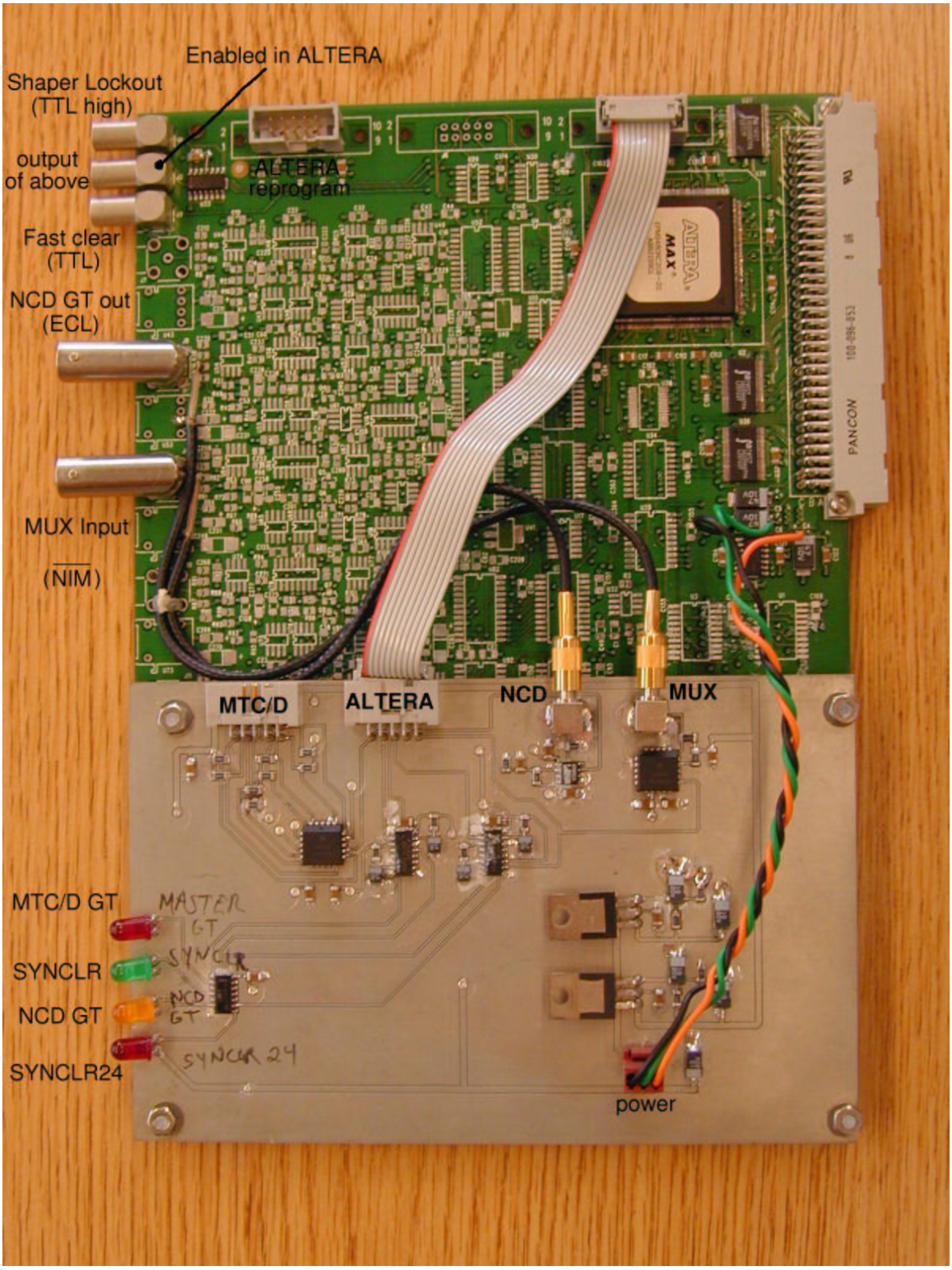

Figure 1: The NCD GTID / Clock Card.